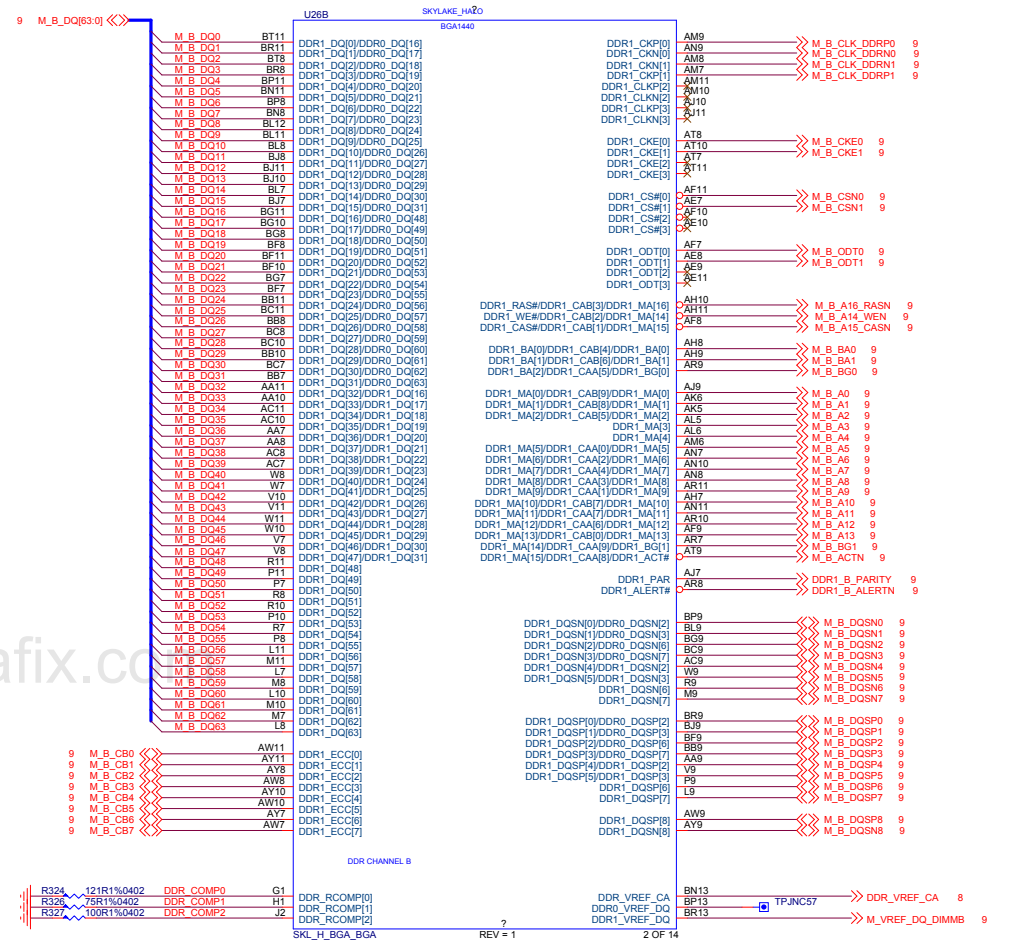
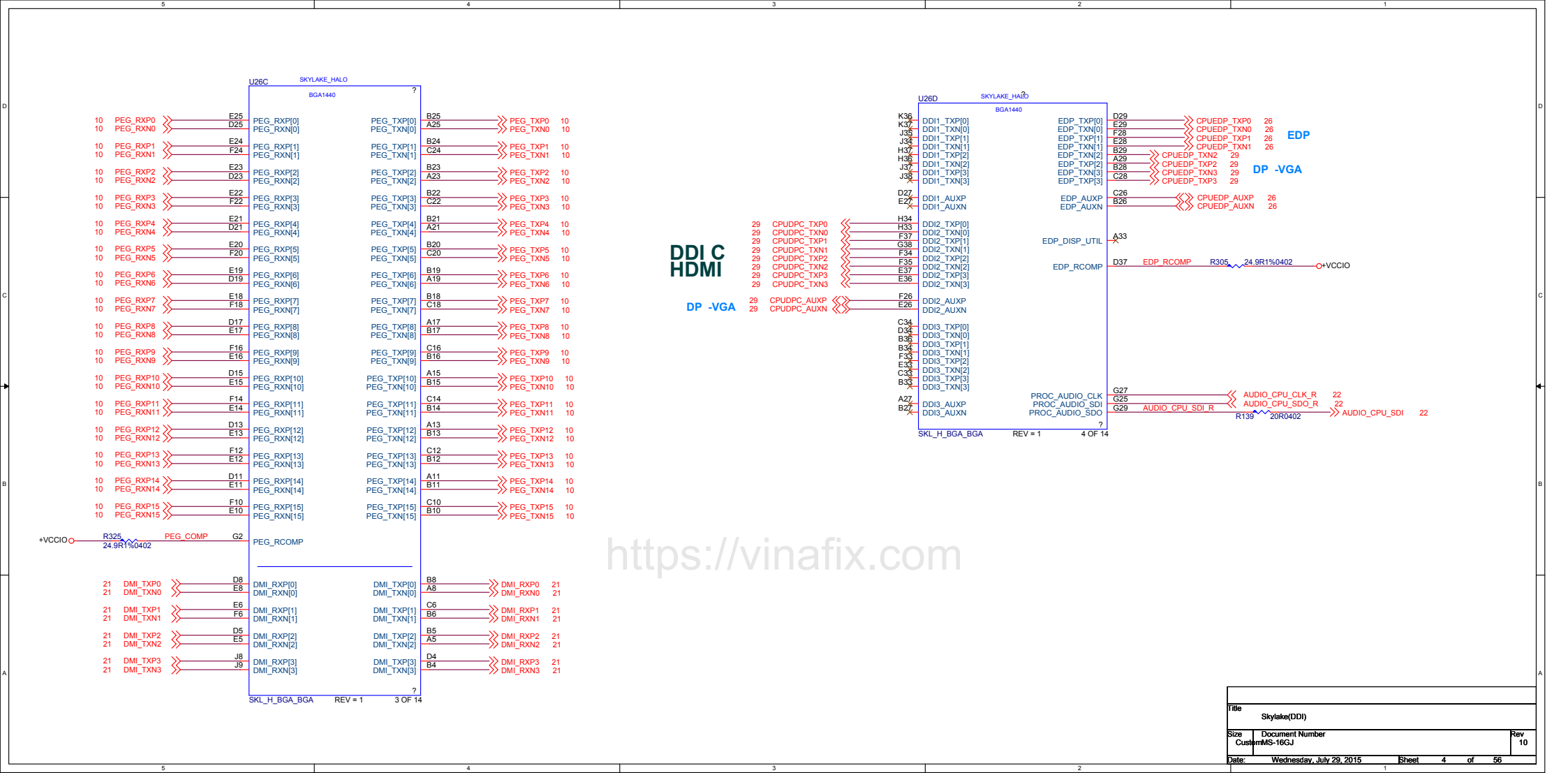


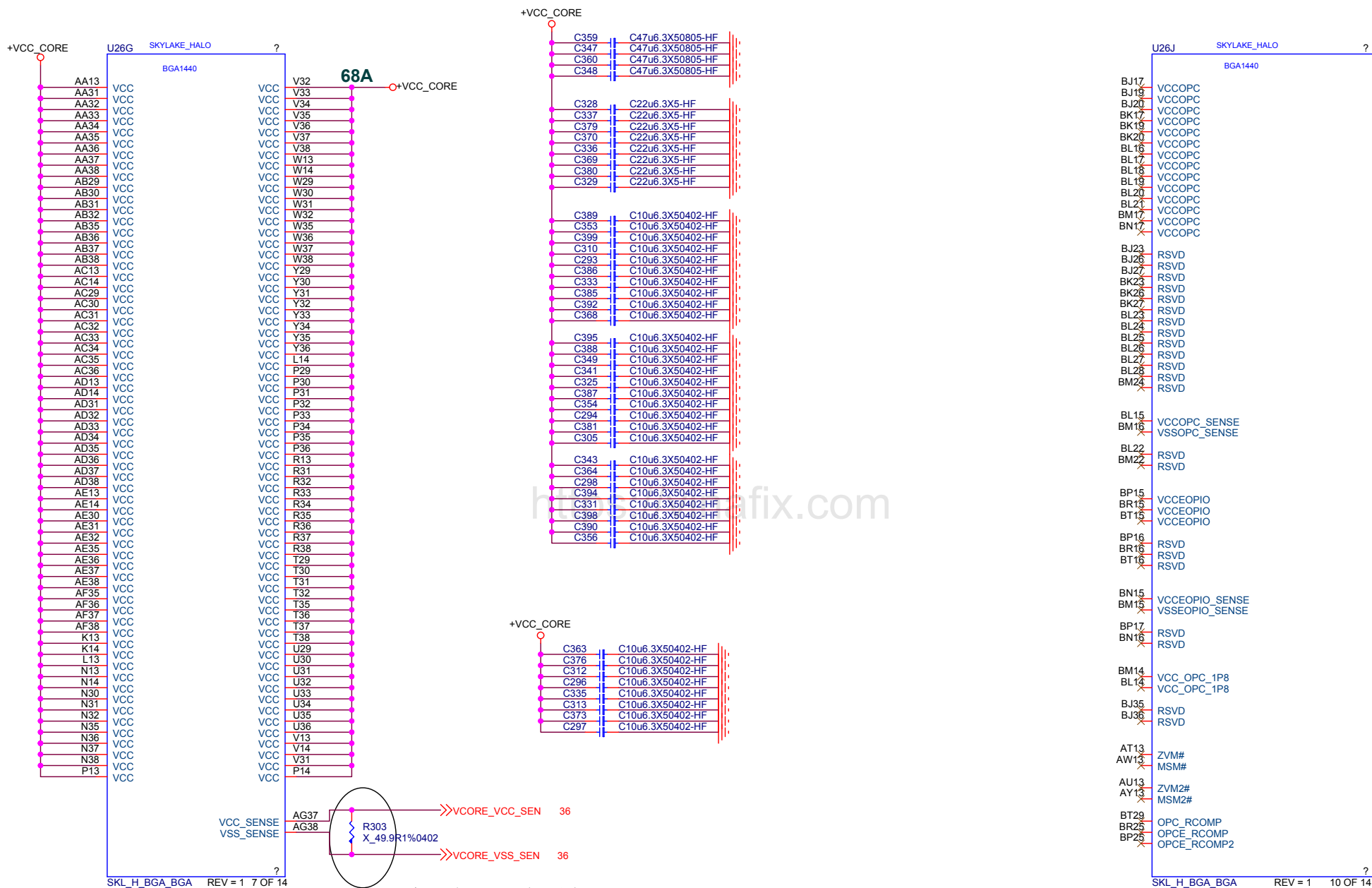


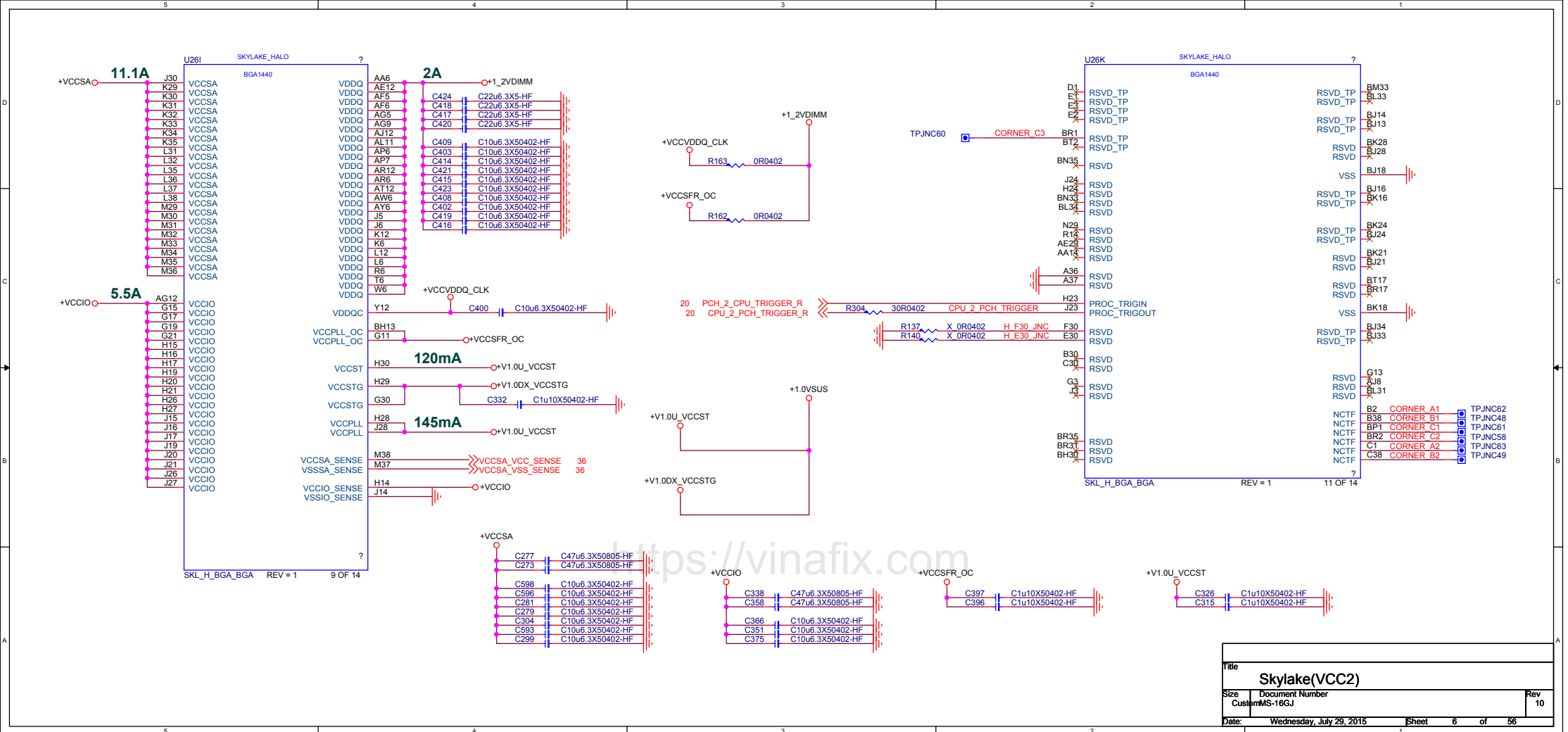
## DDR Channel B

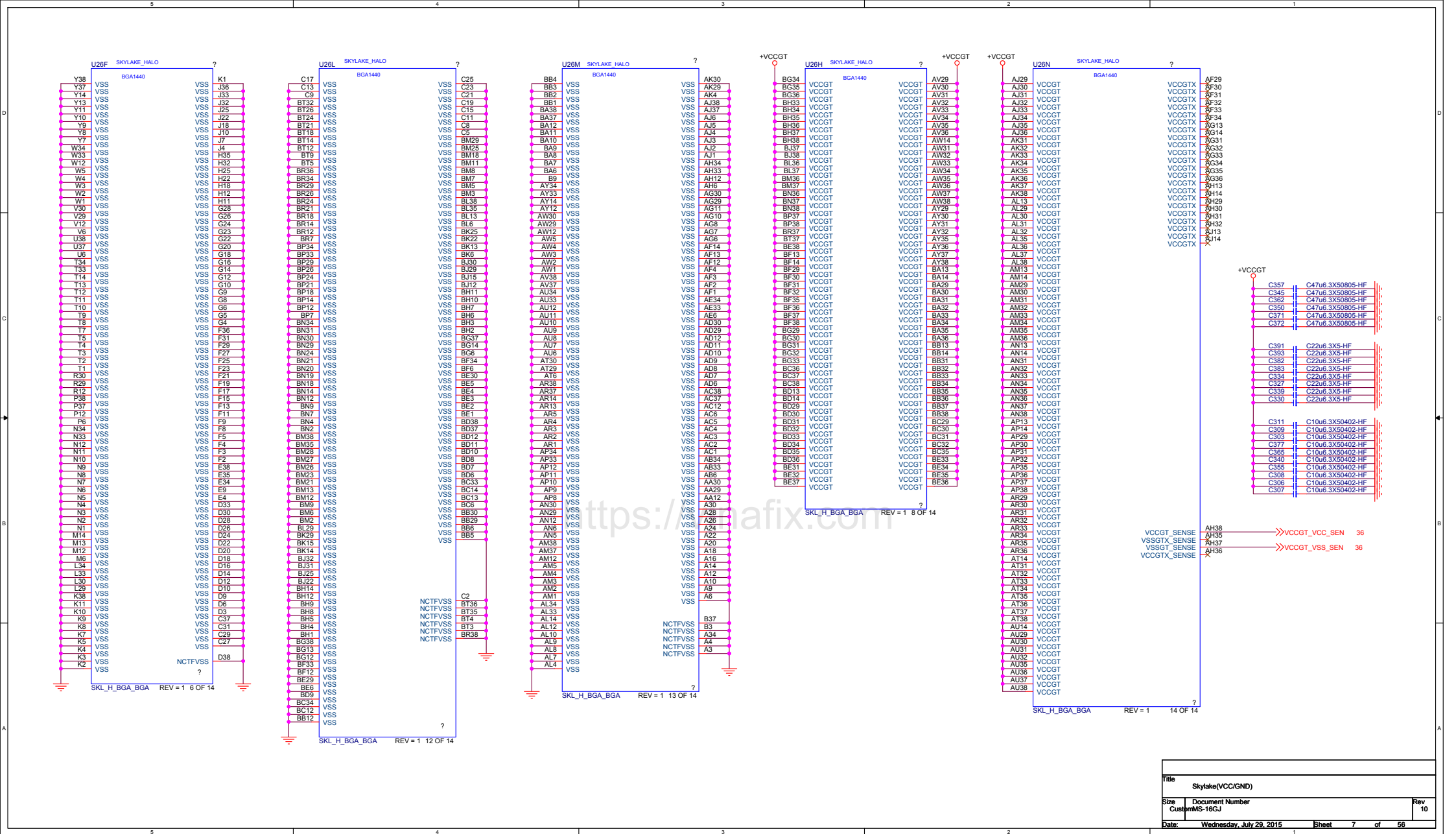


Title			
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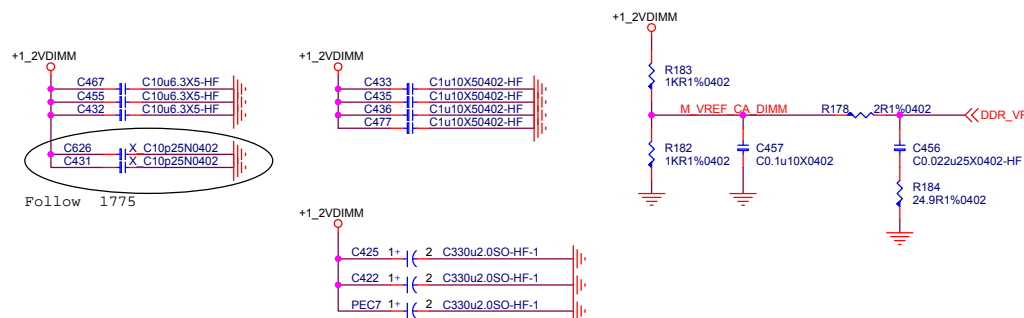
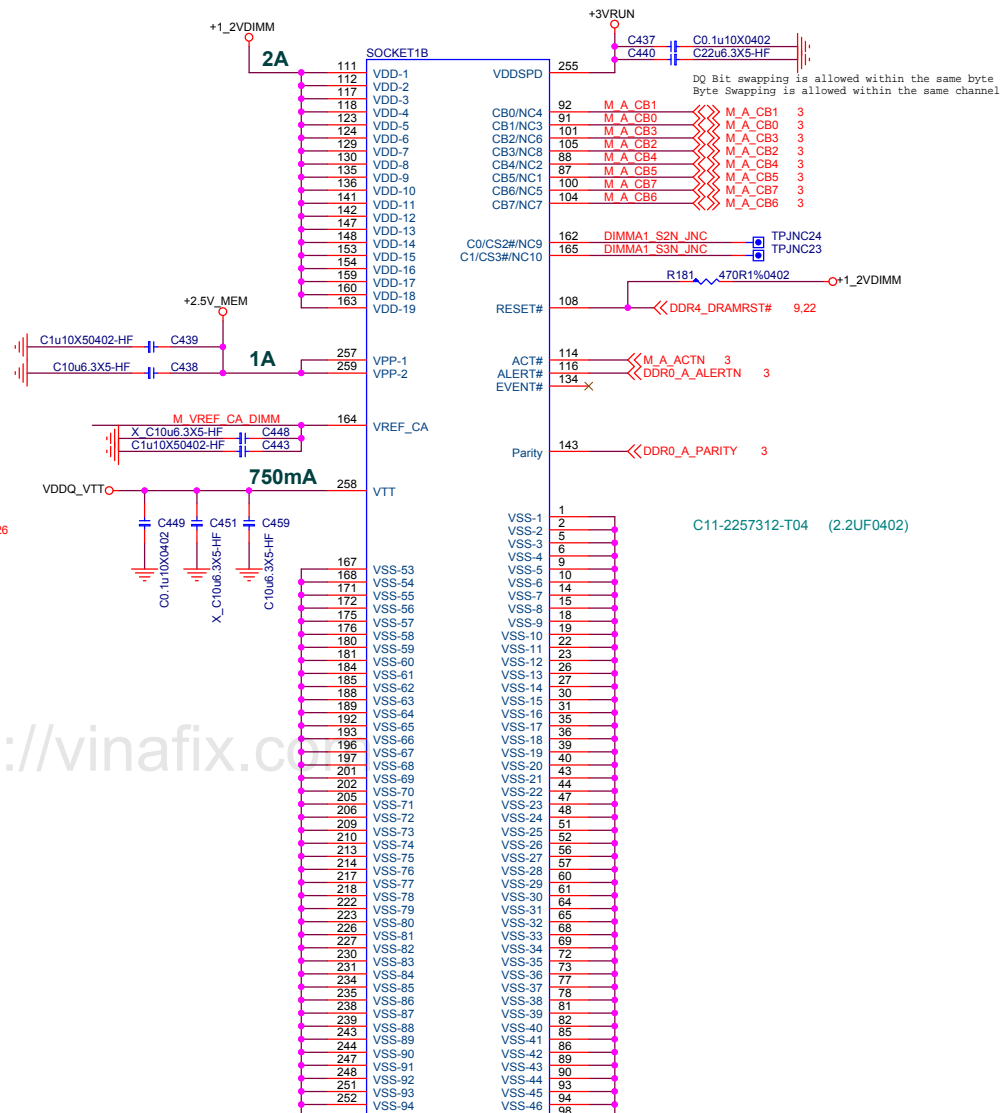
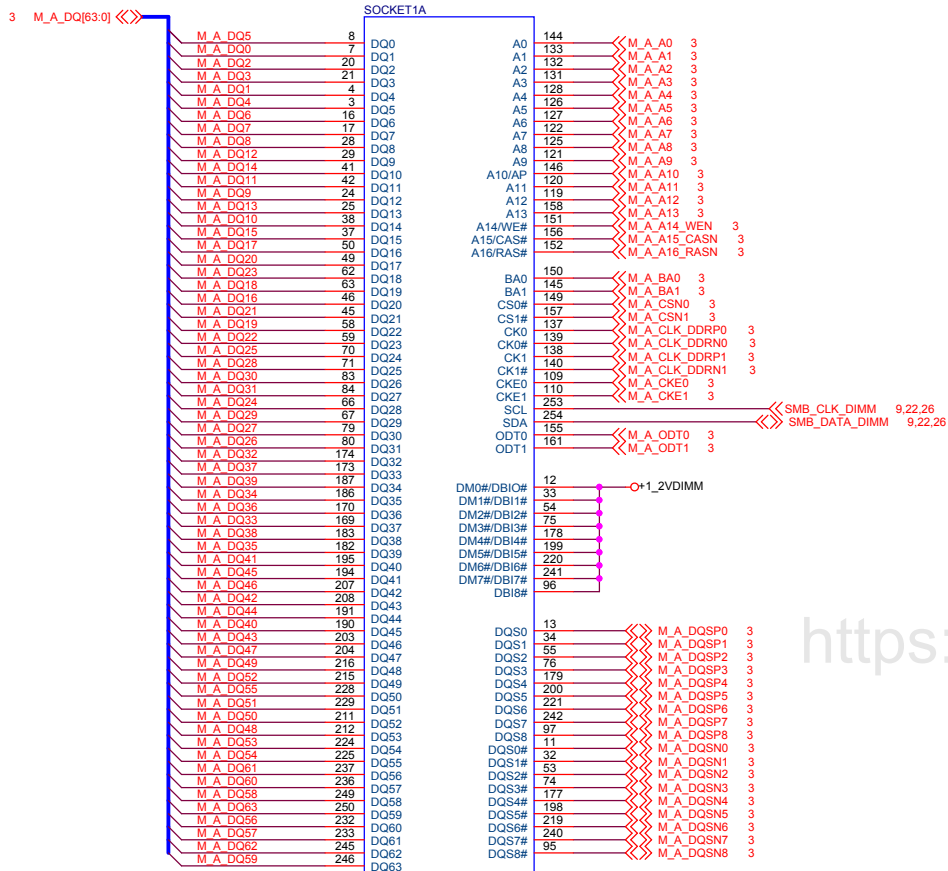








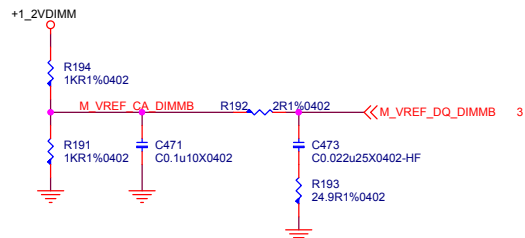
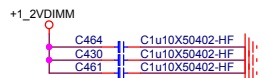
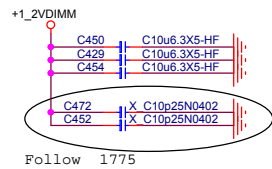
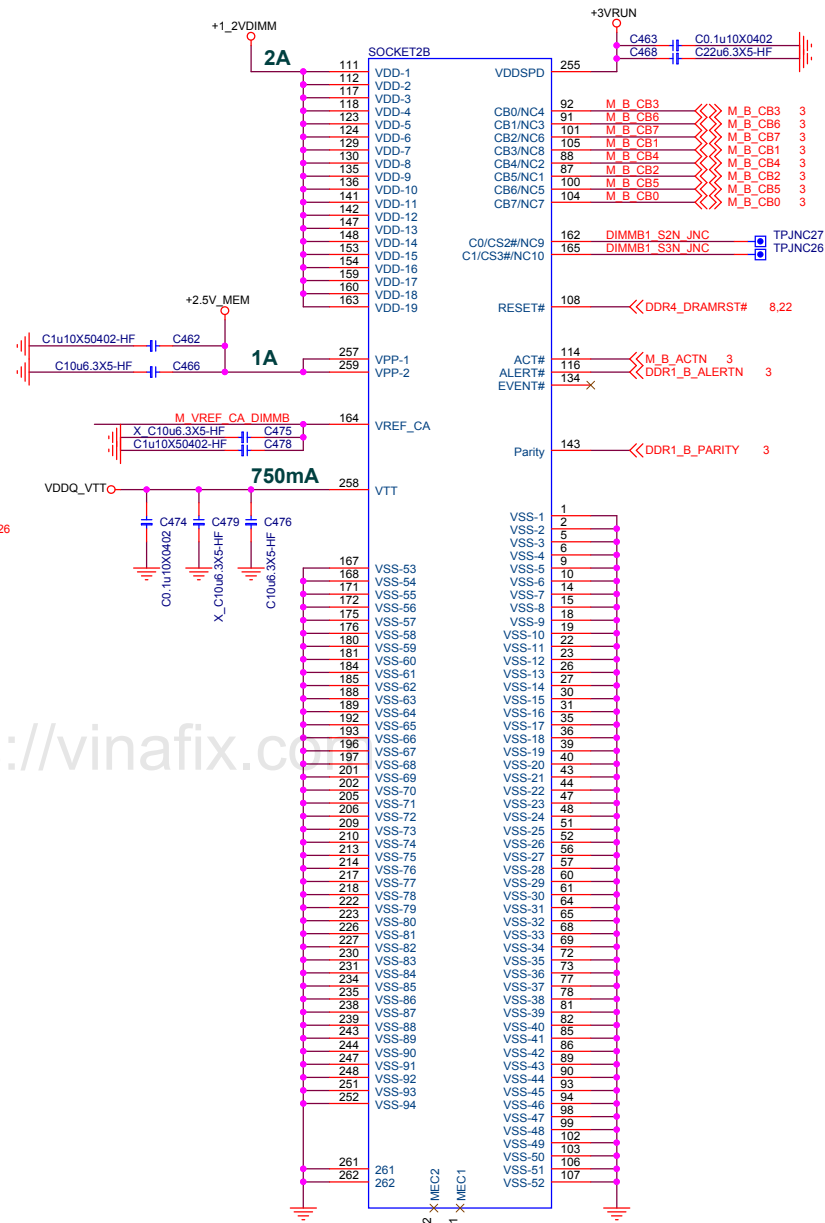
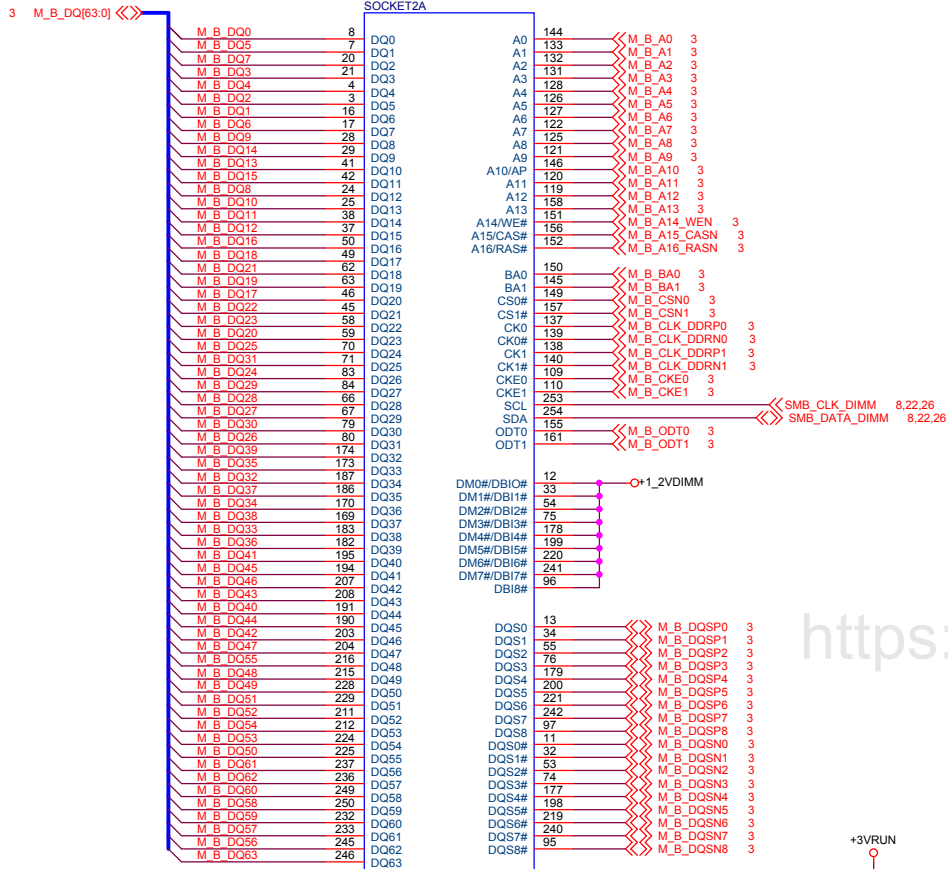
# SODIMM\_A1 (BOT-Reverse)



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DDR4A			
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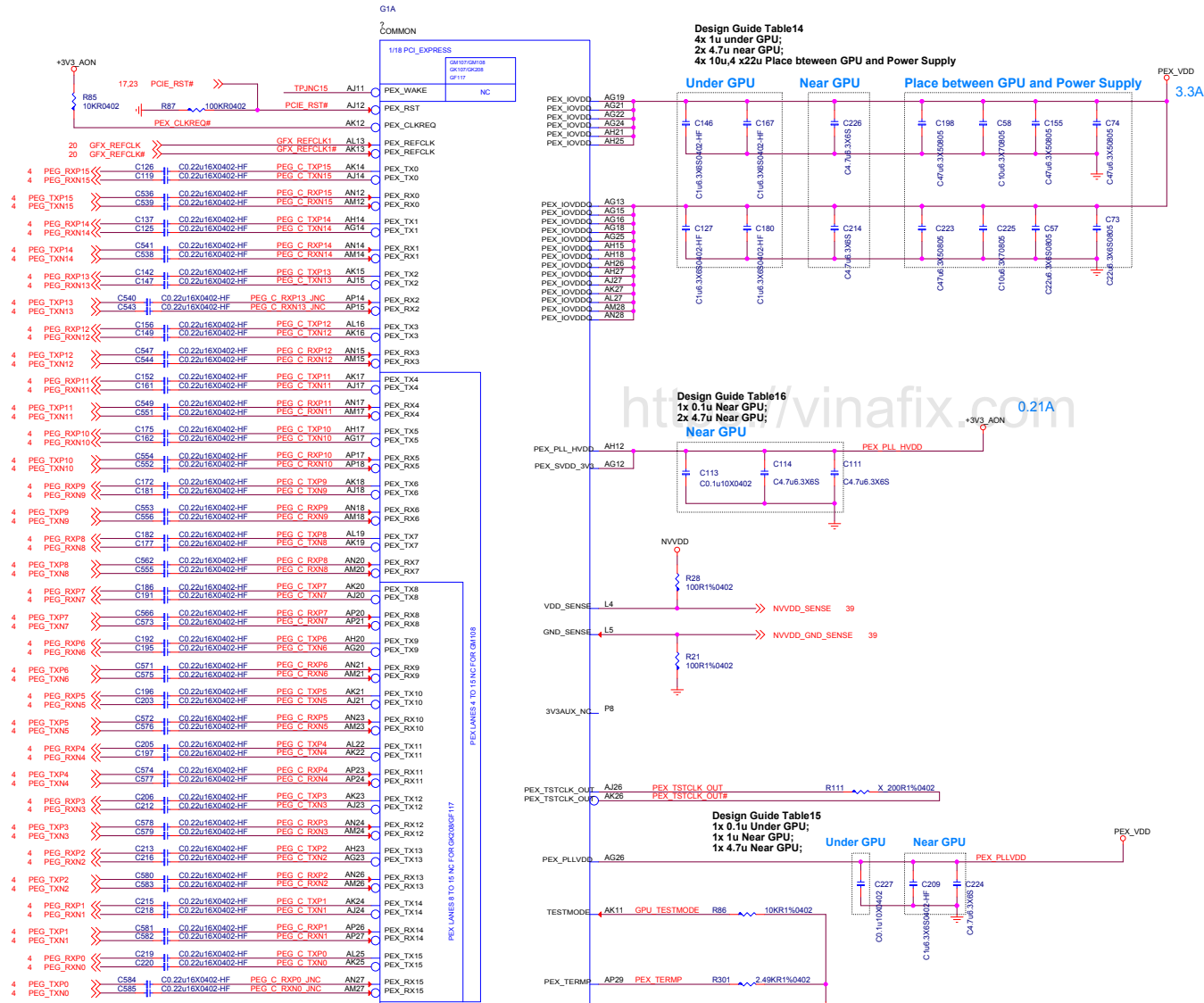
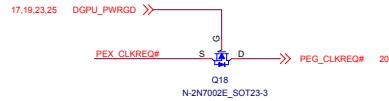
# SODIMM\_B1 (BOT-Reverse)



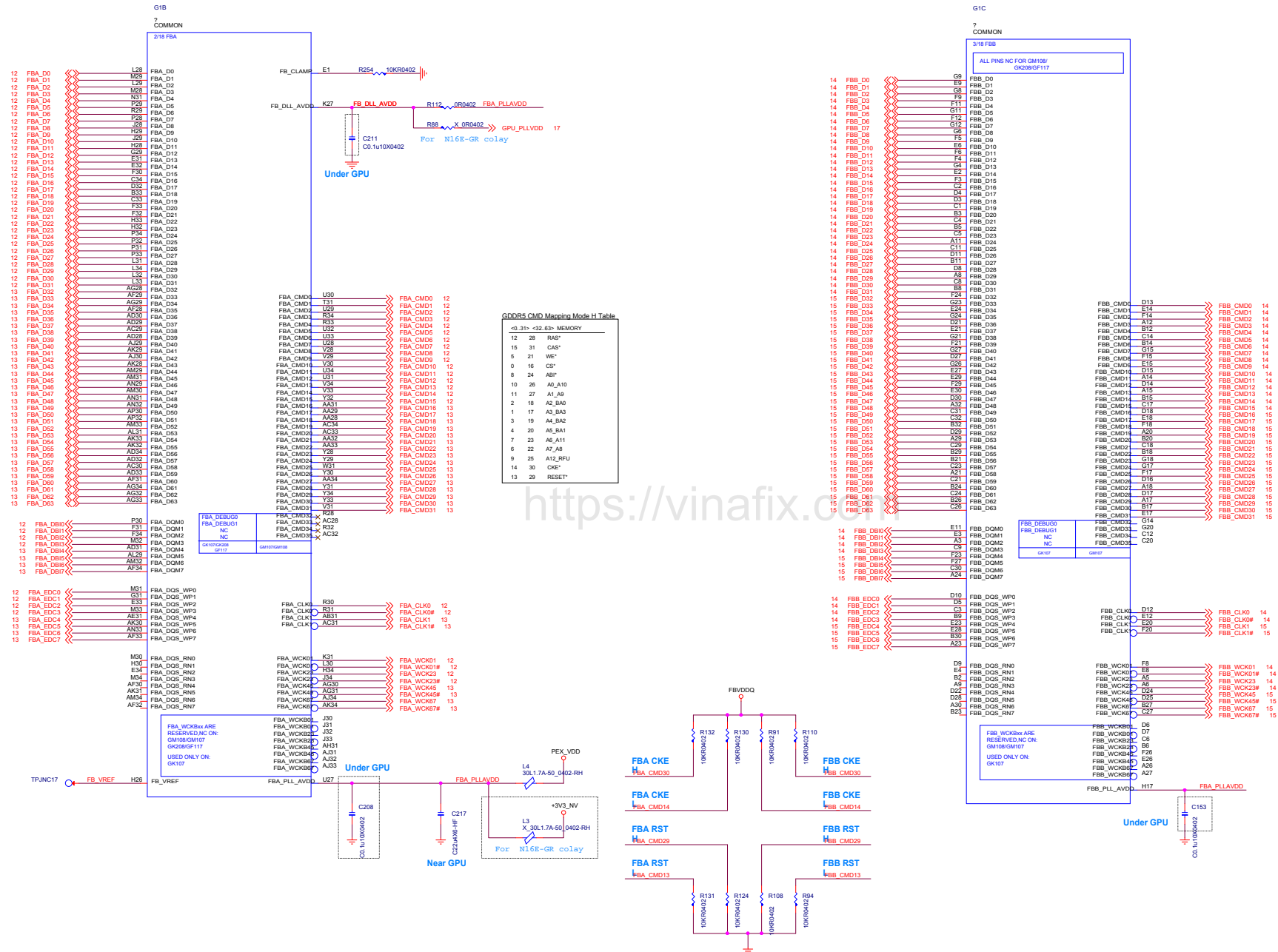
Title		
DDR4B		
Size	Document Number	Rev
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**N16P-GT( PCI-Express Gen3 x16 Interface)**

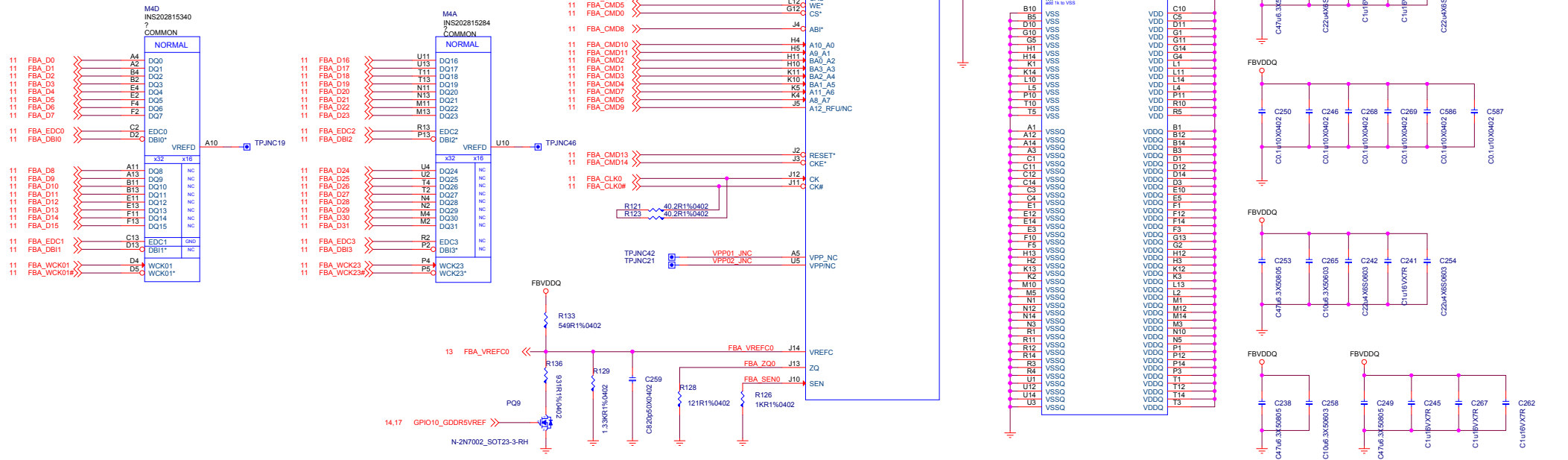
## GPU CLK REQ#



## N16P-GT( Frame Buffer Interface )

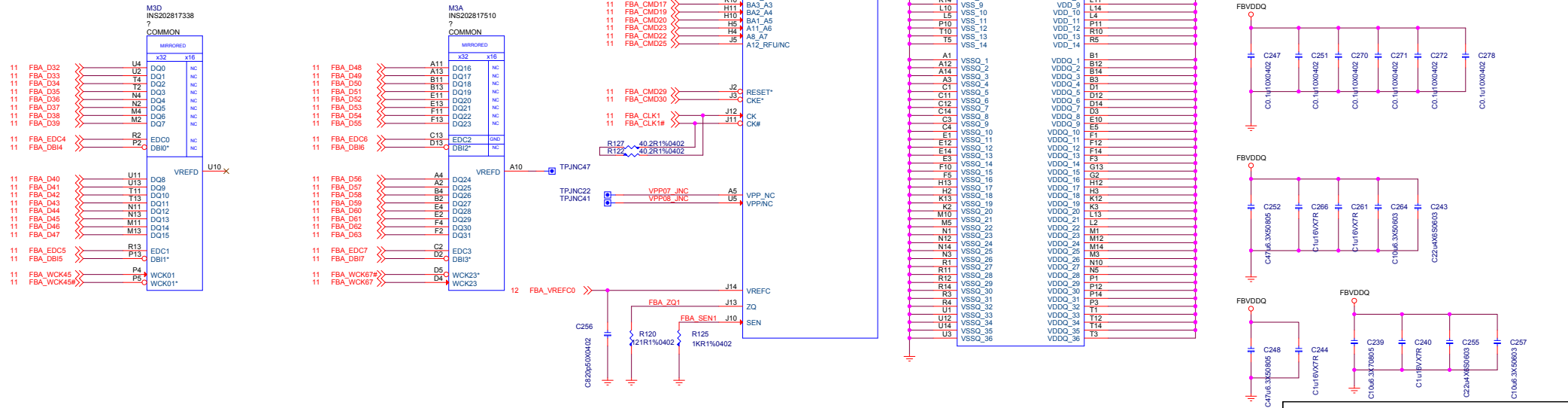


**N16P\_GT( GDDR5 Frame A-1 )**



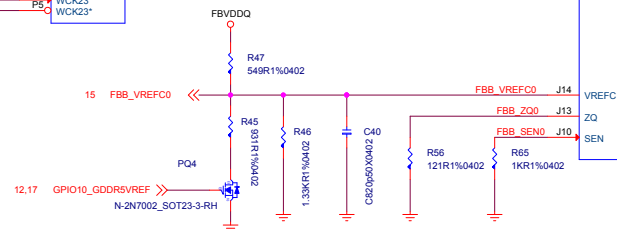
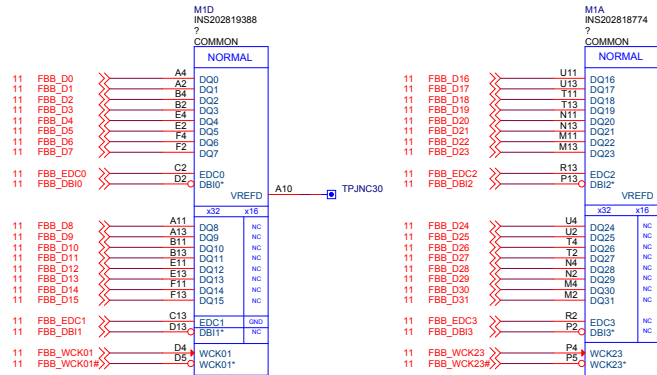
Title				N16P-GT_GDDR5 Frame A-1			
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N16P\_GT( GDDR5 Frame A-2 )



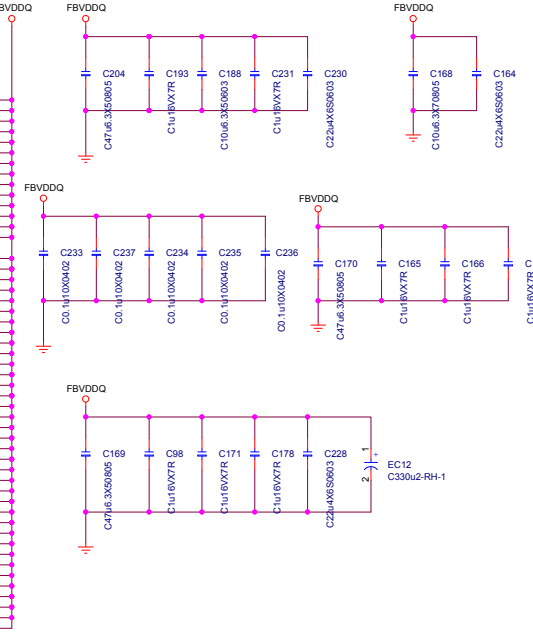
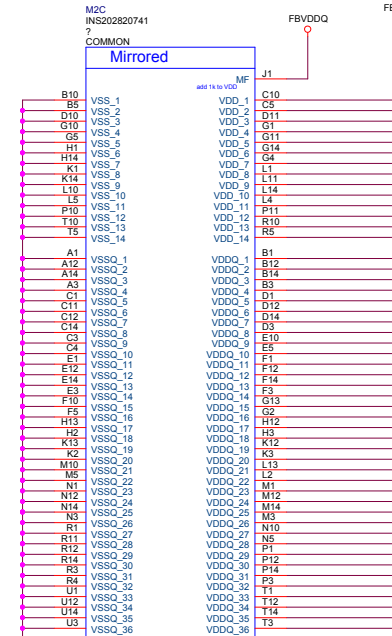
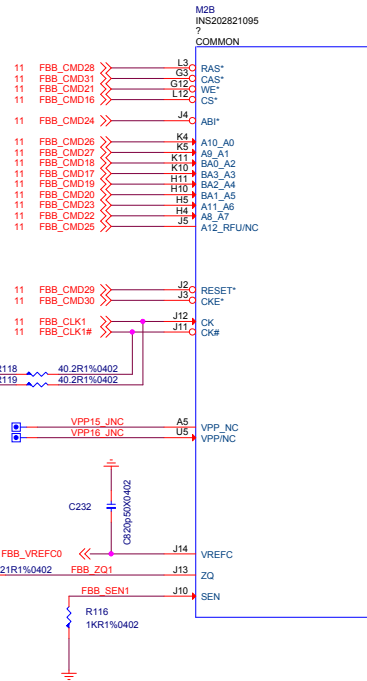
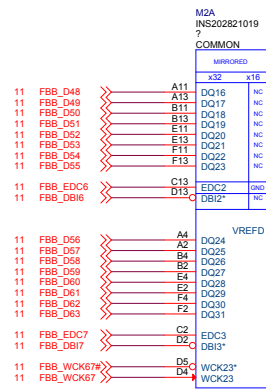
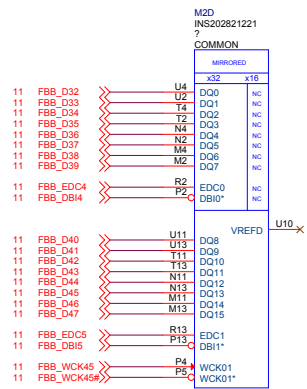
Title				N16P-GT_GDDR5 Frame A-2			
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# N16P\_GT( GDDR5 Frame B-1 )



<https://vinafix.com>

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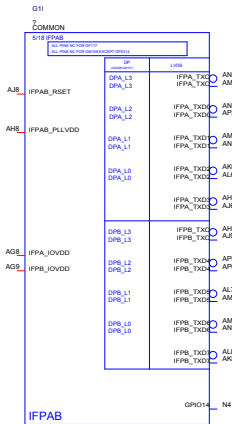


<https://vinafix.com>

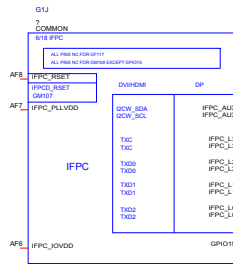


N16P-GT( Display IF)

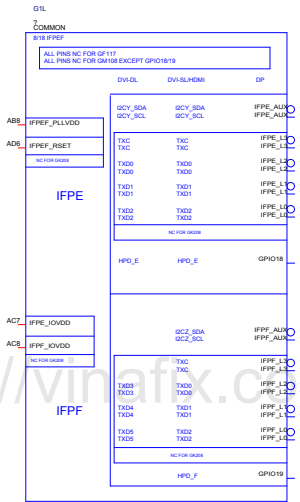
IFP A/B LVDSDual Link



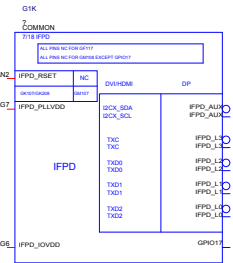
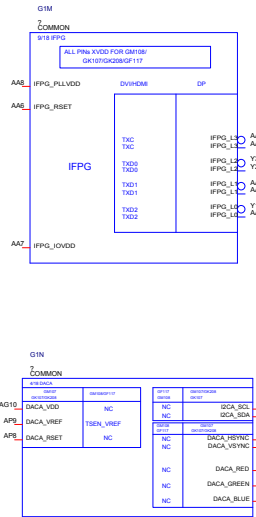
IFP C Native HDMI OR DP

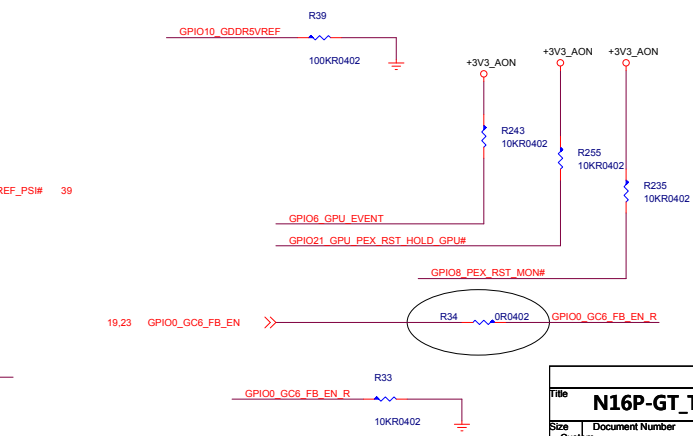
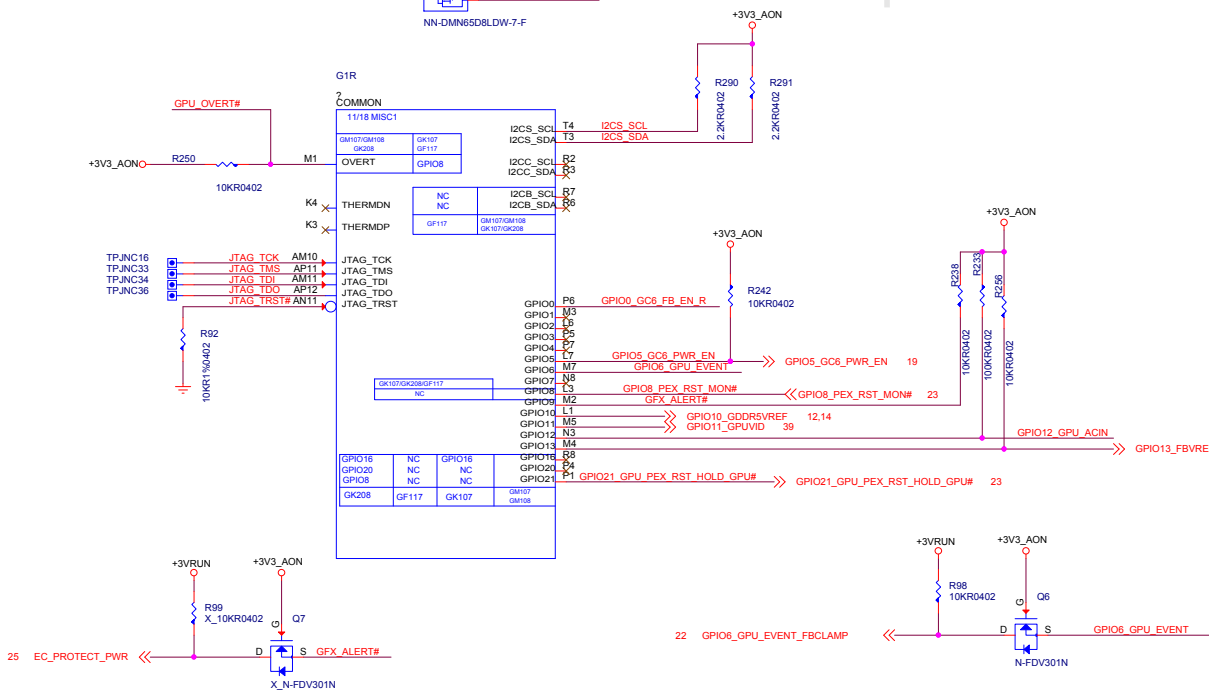
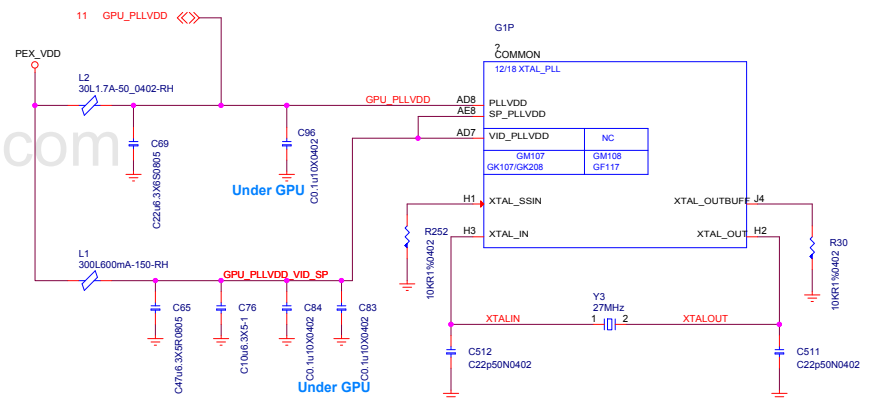
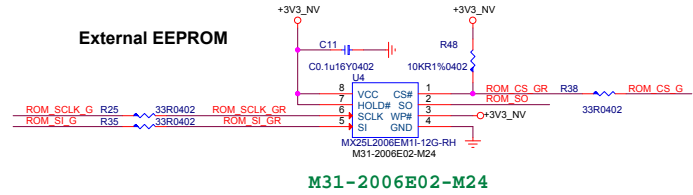
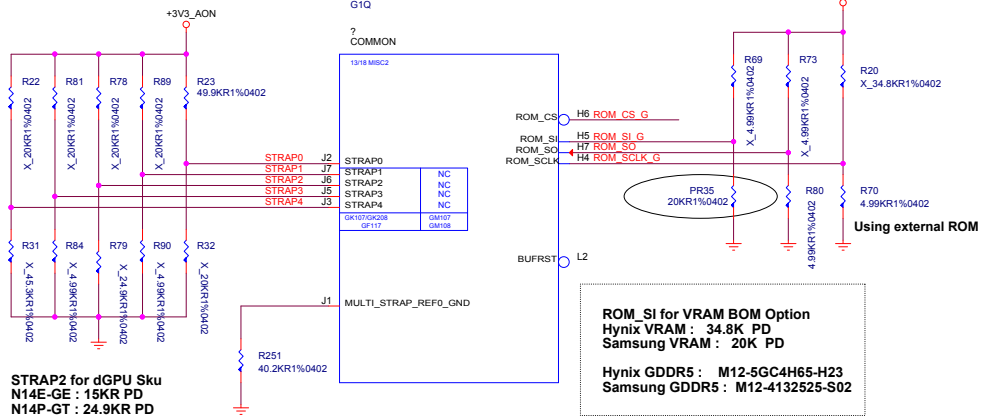
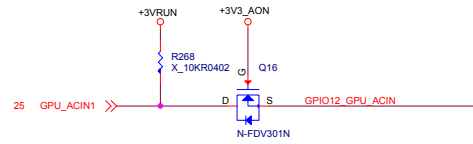
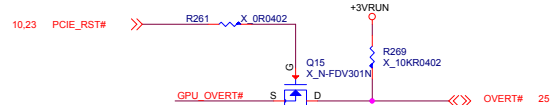
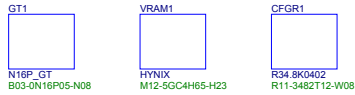


IFP E/F Dual Link TMDS DVI-I

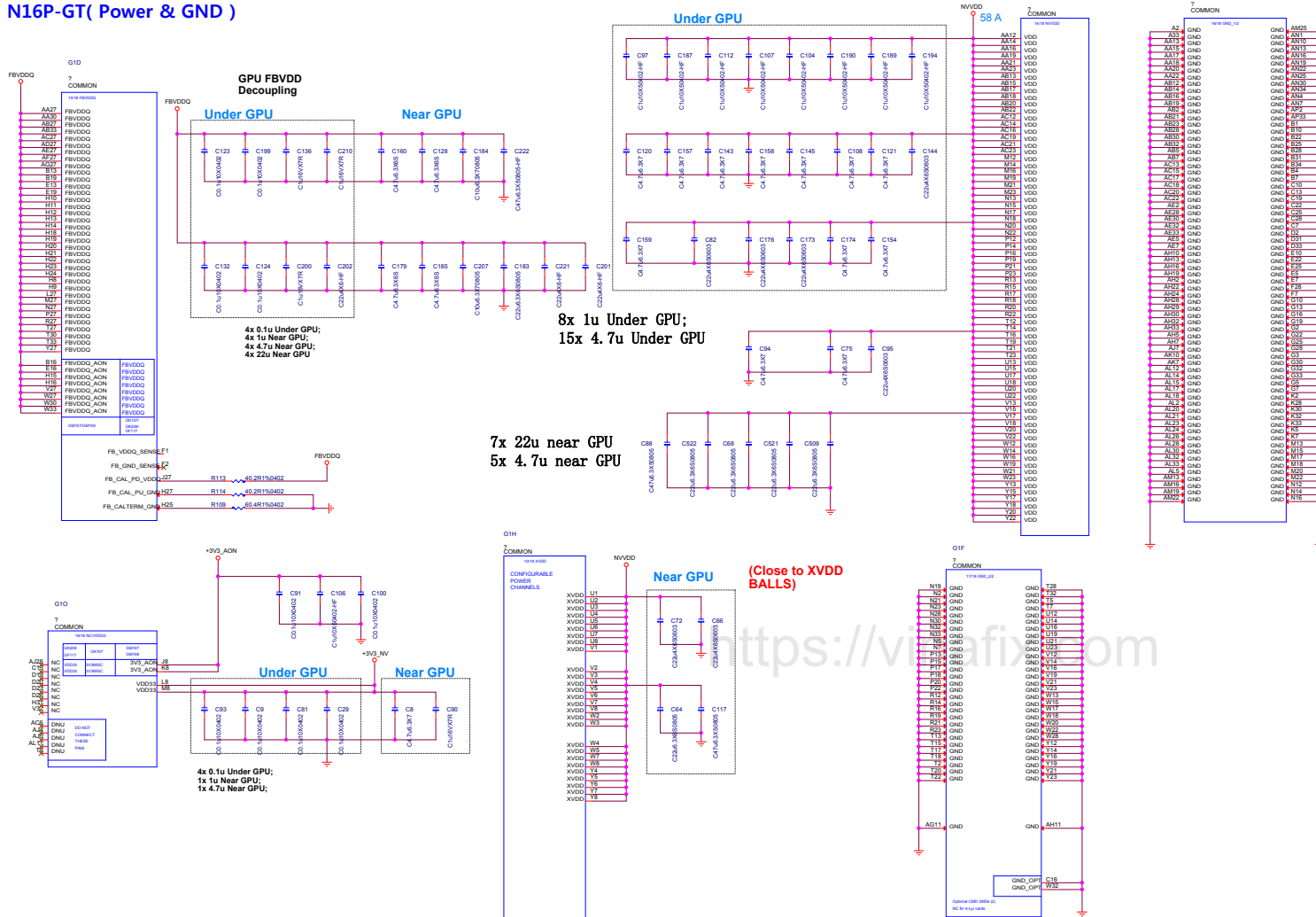


DAC A VGA



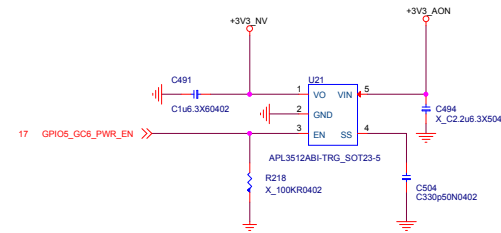


## N16P-GT( Power & GND )

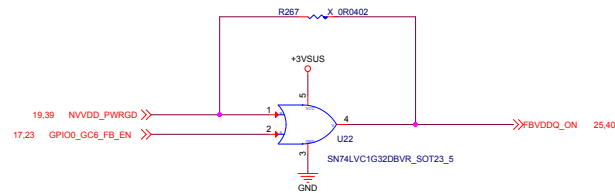


**+3V3\_AON -> +3V3\_NV -> NVVDD -> PEX\_VDD -> FBVDDQ -> DGPUPWRGD**

The schematic diagram illustrates the power management section for the i6508LDW-7-F\_SOT363-6. It shows the connection of the PLT\_RST# pin to the 3V3\_NV supply. Key components include resistors R328 (0R0402), R332 (0R0603), and R333 (0R0402), and capacitors C503 (3X60603) and C504 (3X60603). The diagram is annotated with 'add PLT\_RST# to avoid 3V3\_NV Leakage' and 'Disable GC6'.

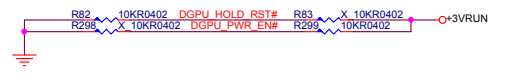
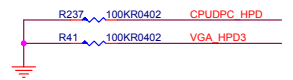
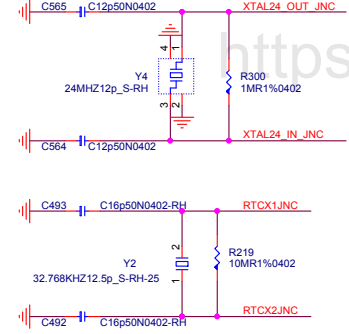
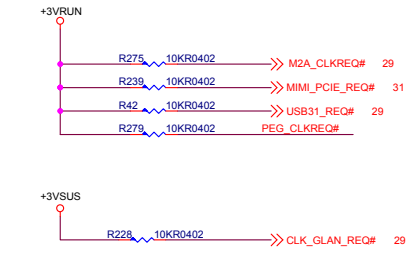


## Disable GC6

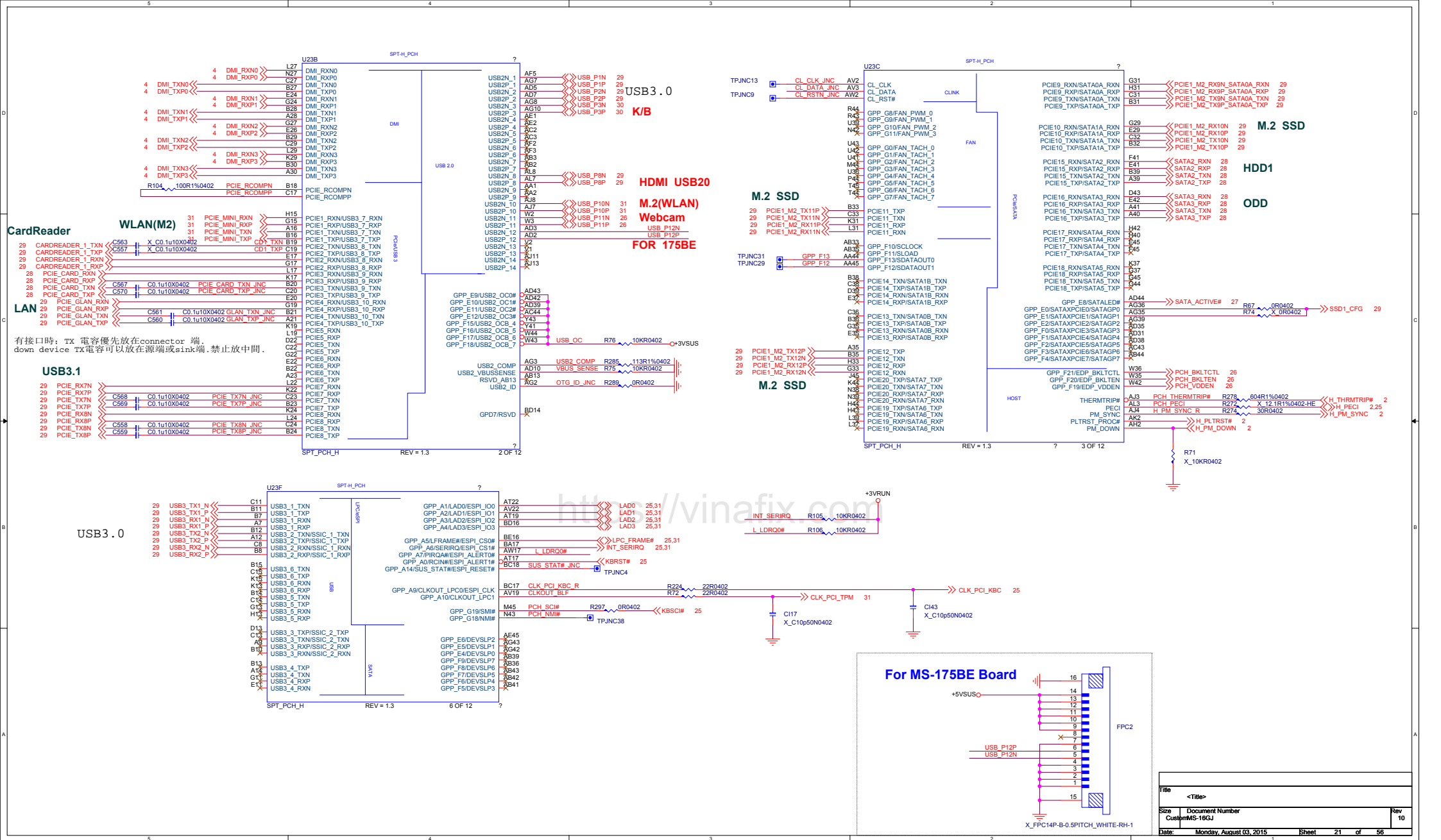
[illegible][illegible]

For 175B  
cardreader  
小板上拉電阻

CLKREQ#靠近 device端放置。



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有接口時: TX 電容優先放在connector 端.  
down device TX電容可以放在源端或sink端.禁止放中間.

LAN

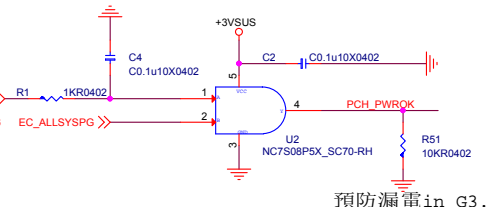
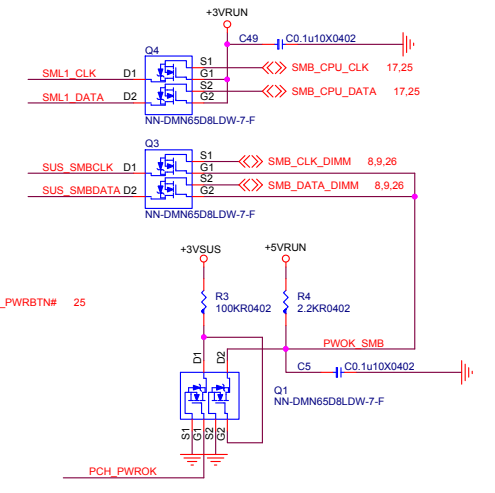
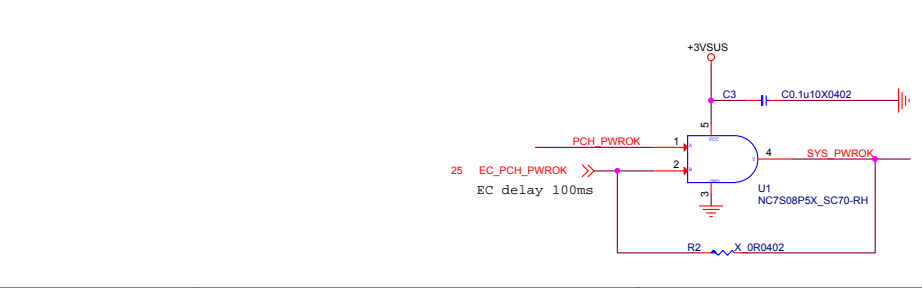
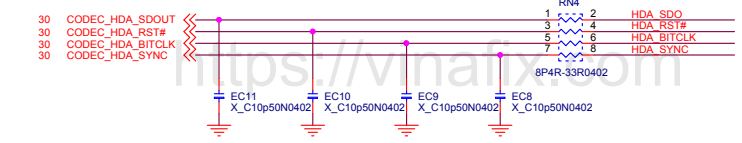
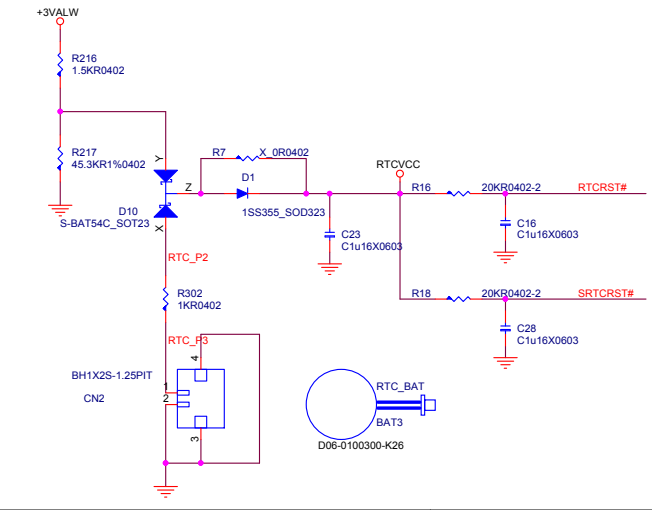
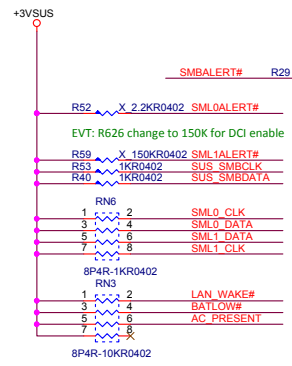
USB3.1

USB3.0

For MS-175BE Board

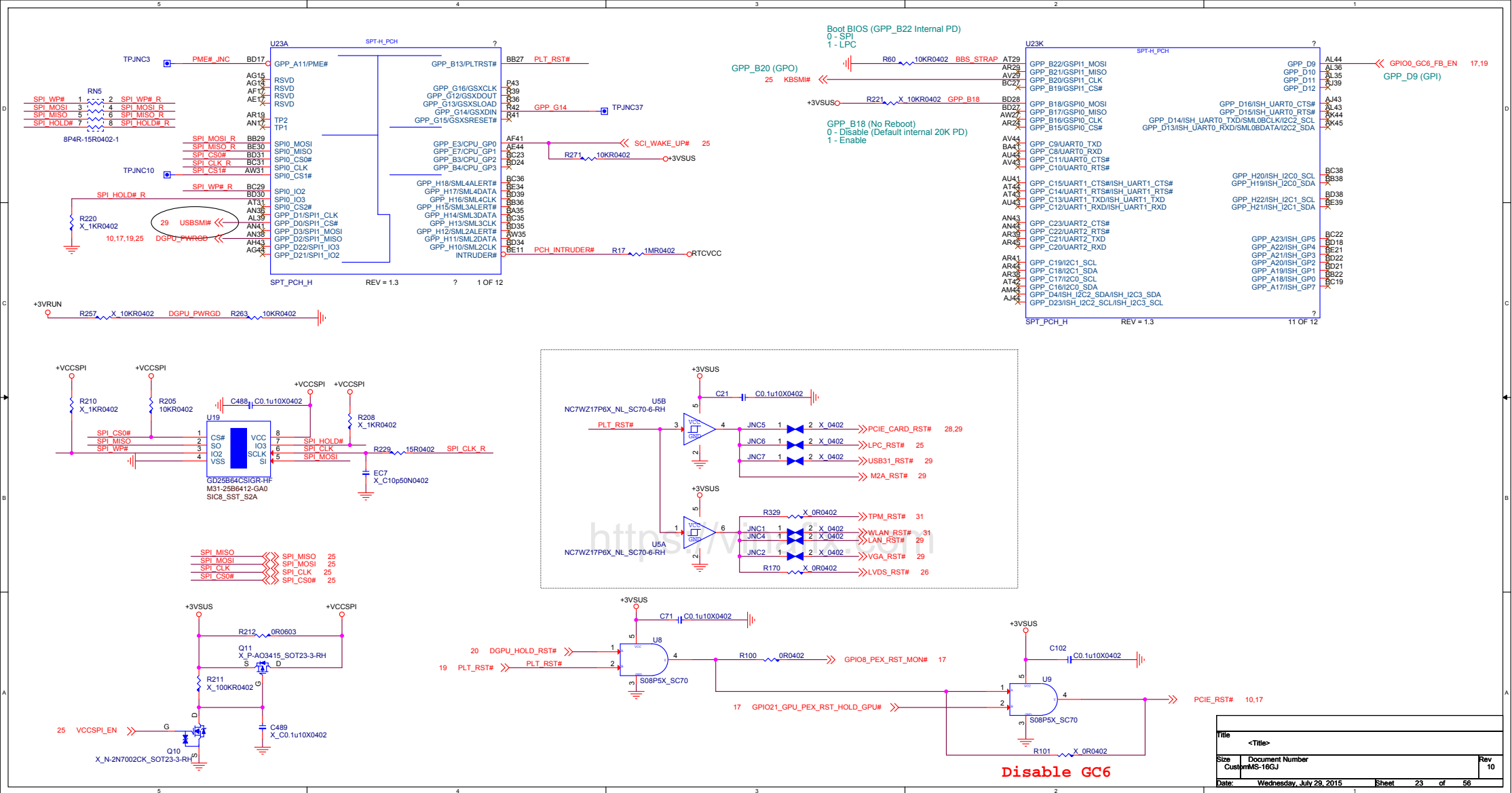
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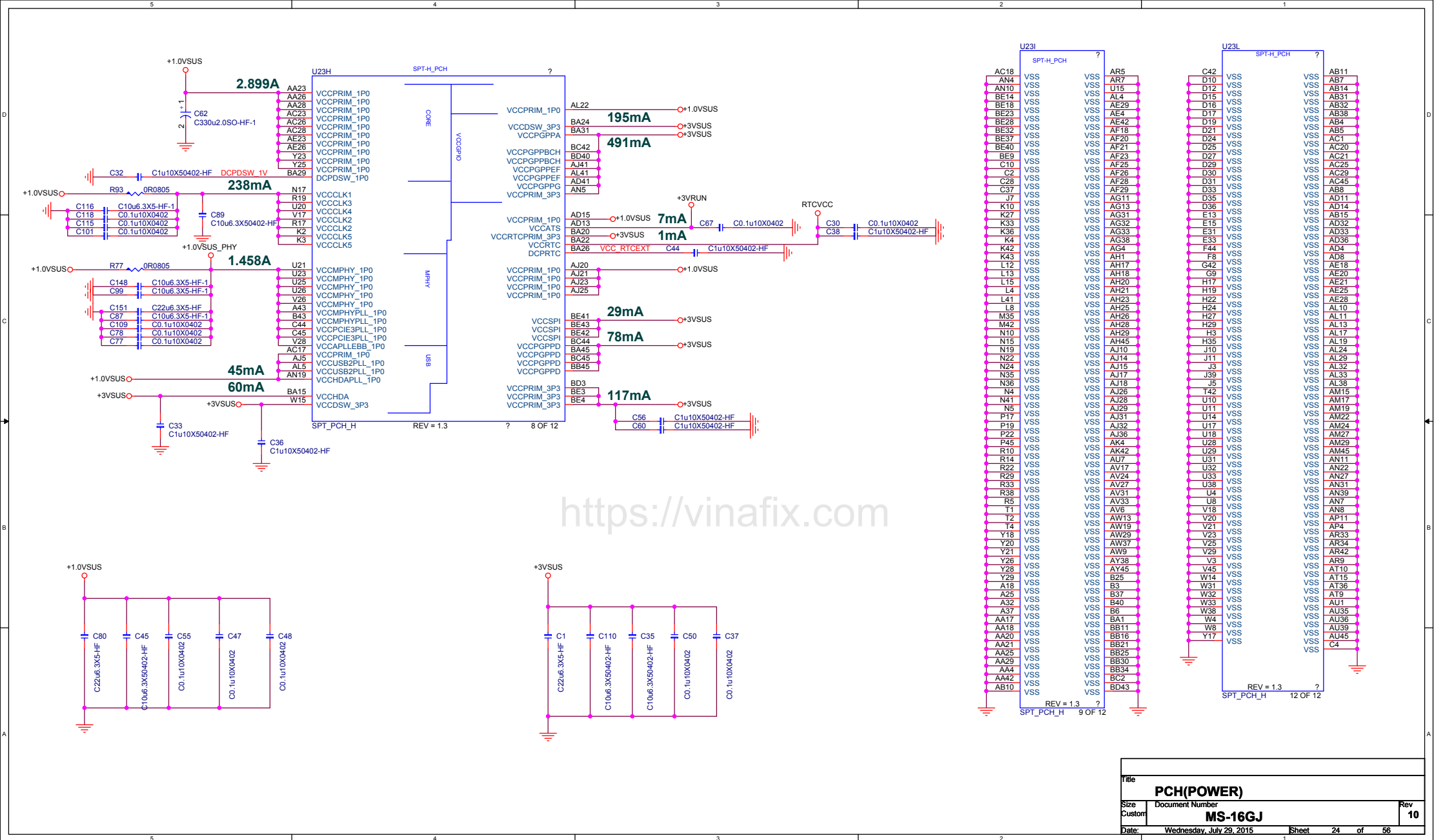
SMBALERT#  
0 - Disable (Default Internal 20K PD)  
1 - Enable (AMT/SBA)  
SML0ALERT#  
0 - LPC (Default Internal 20K PD)  
1 - eSPI



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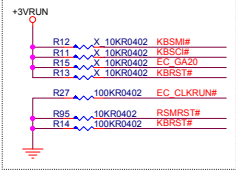




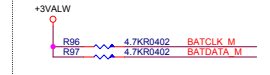
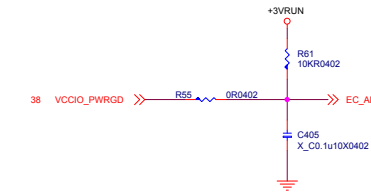
Title				
<b>PCH(POWER)</b>				
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RSMRST# follow DG modify to 10K

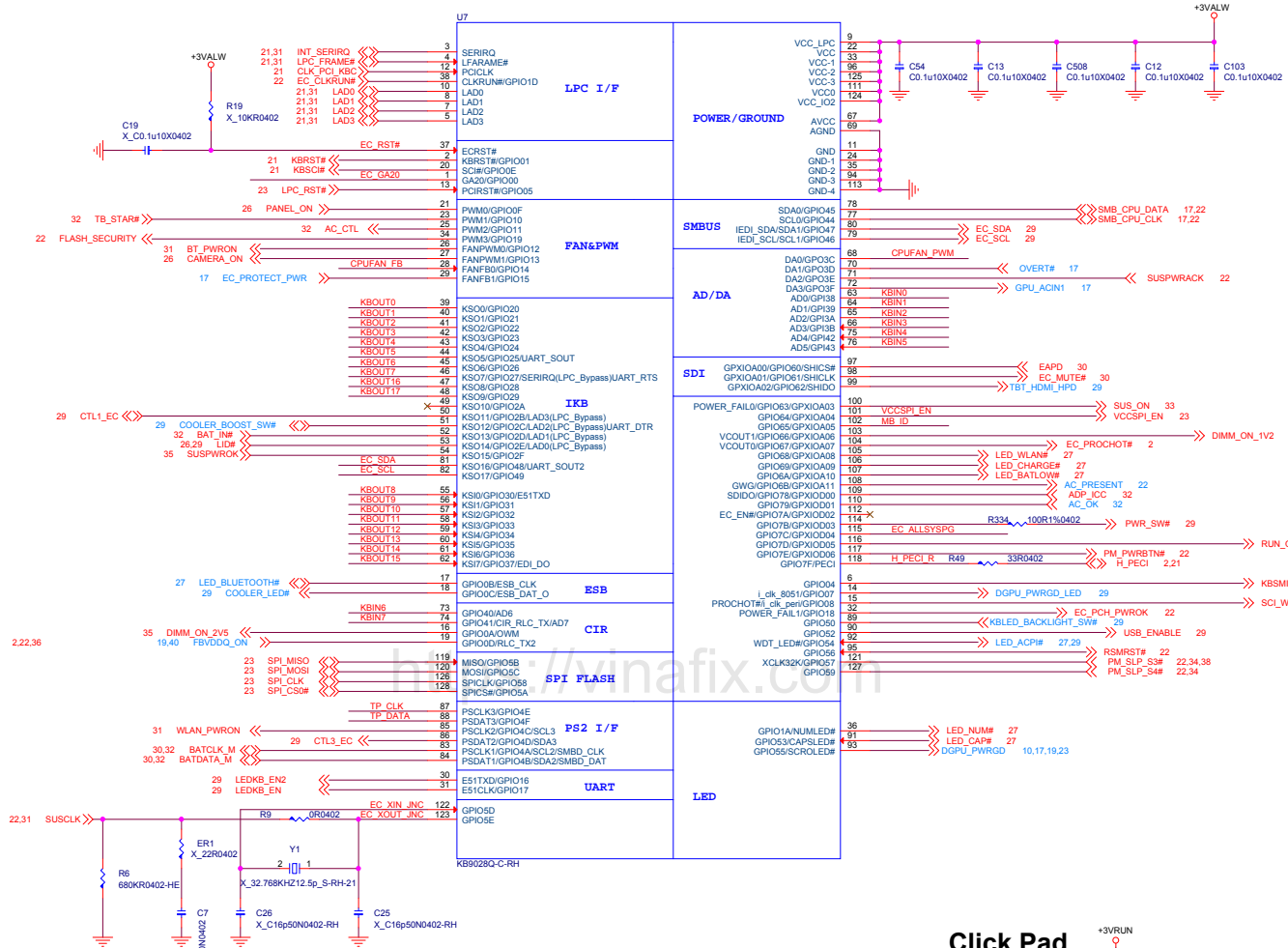
## PU/PD



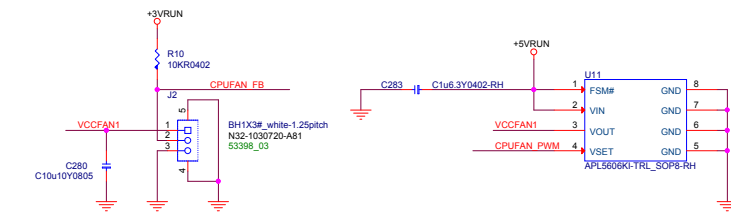
## LID pull hi 10K



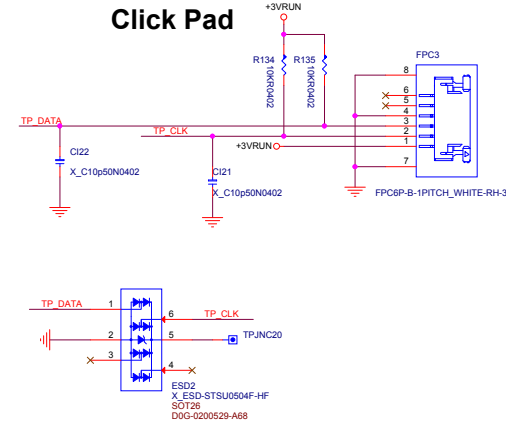
# KBC/EC/uP (ENE9028)



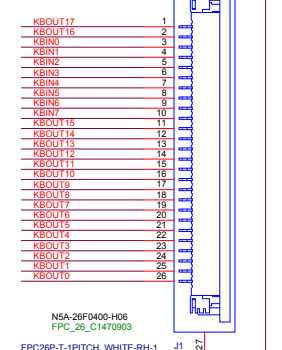
## CPU FAN



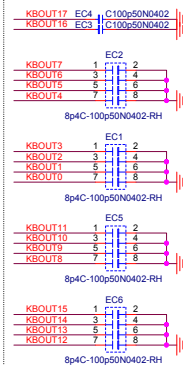
## Click Pad



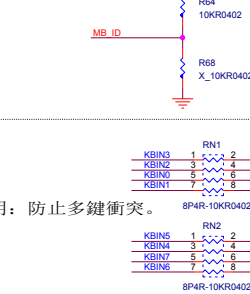
## Keyboard conn



## For EMI



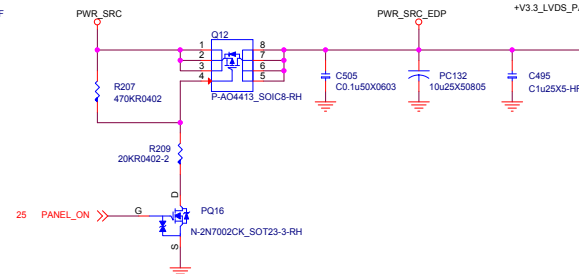
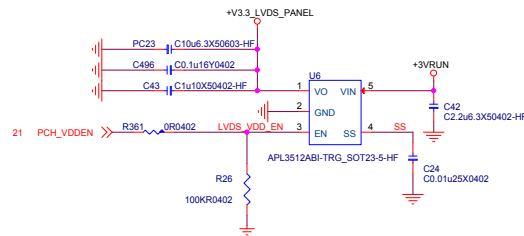
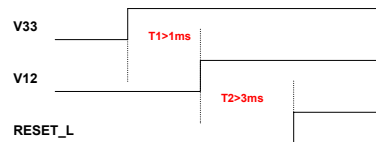
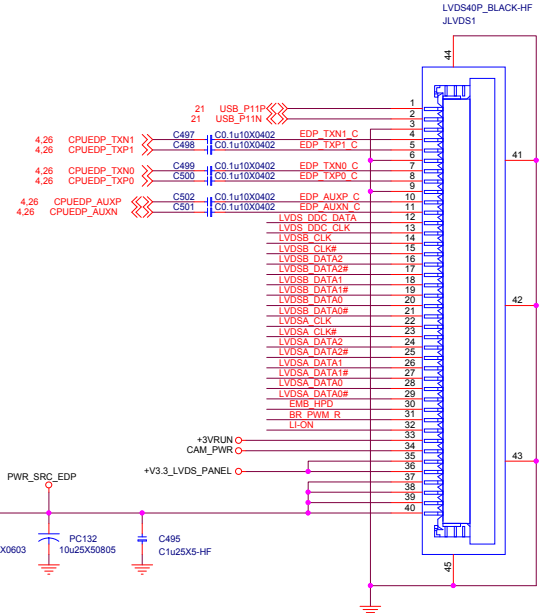
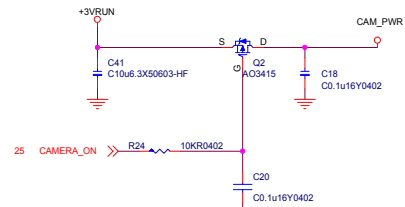
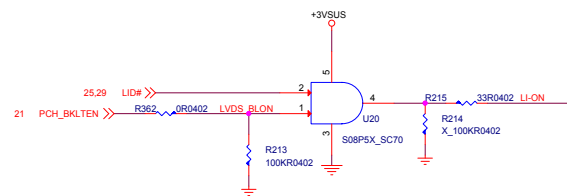
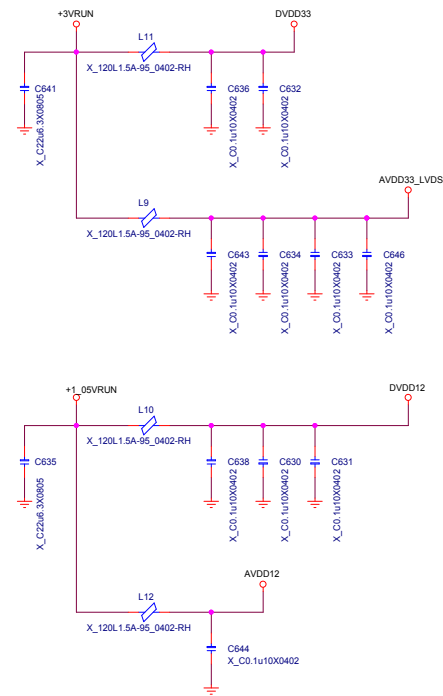
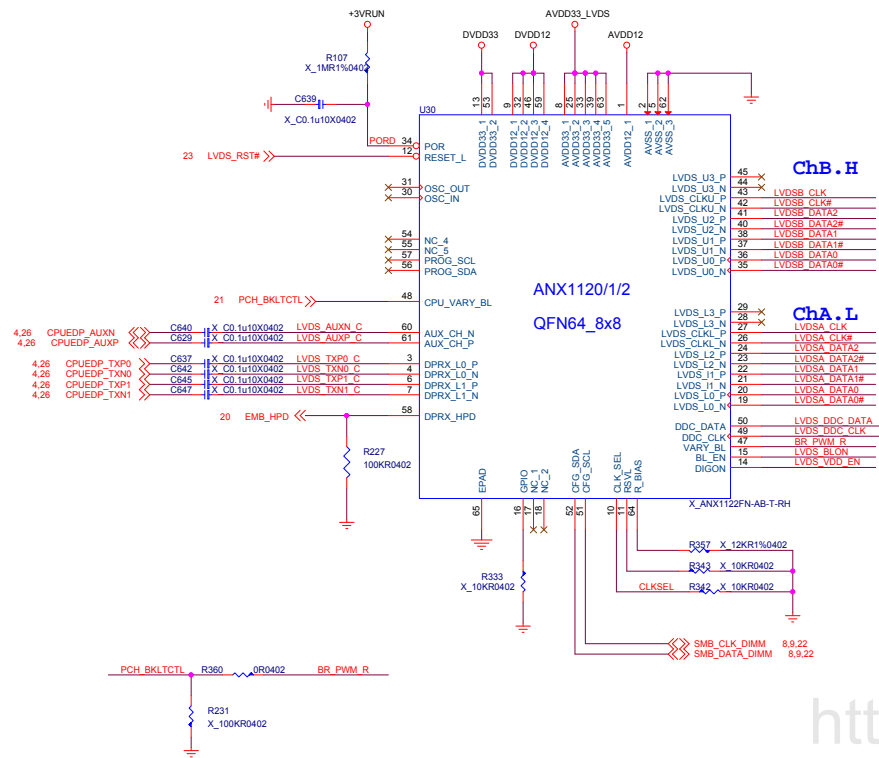
## MotherBoard ID

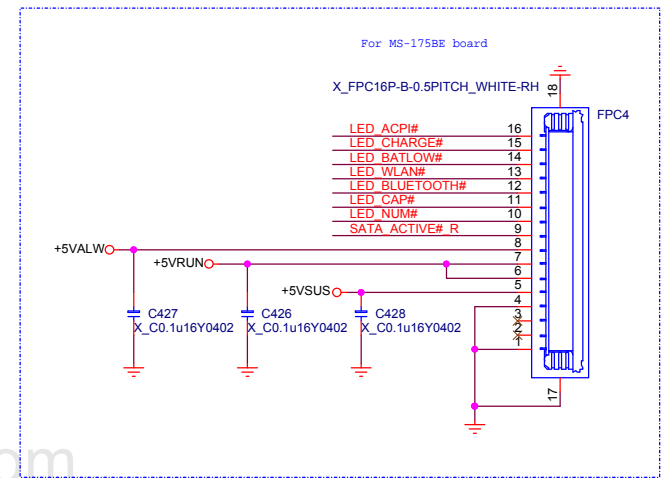
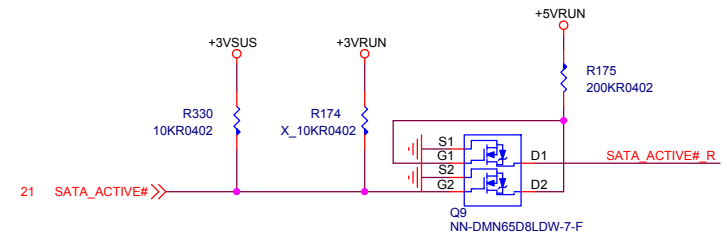
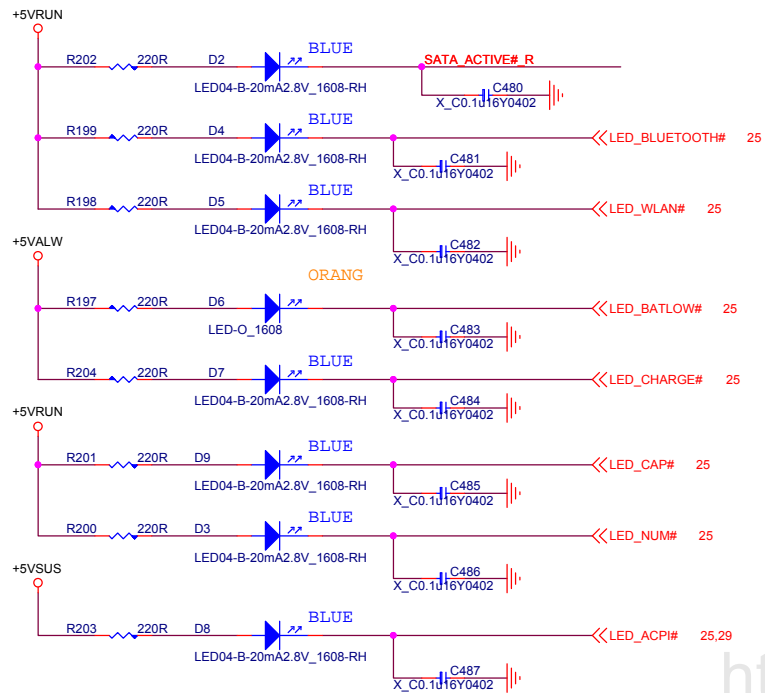


作用：防止多鍵衝突。

EVT: KBIN add 10K pull high to +3VALW for EC request

## eDP to LVDS





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**Pin 13/15/16/22/23/24/25/26 definition  
are different from RTS5227**

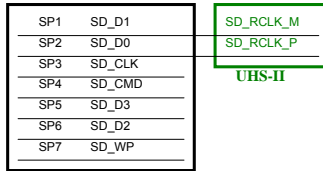
[illegible]

Diagram illustrating the wiring for a SATA to SATA III adapter. The diagram shows the connection of the SATA connector (left) to the SATA III connector (right).

**SATA Connector (Left):**

- Pin 1: C625 (0.01u25X0402) SATA3TXP\_C\_JNC
- Pin 2: C622 (0.01u25X0402) SATA3TXN\_C\_JNC
- Pin 3: C621 (0.01u25X0402) SATA3RXN\_C\_JNC
- Pin 4: C618 (0.01u25X0402) SATA3RXP\_C\_JNC

**SATA III Connector (Right):**

- Pin 1: GND
- Pin 2: GND
- Pin 3: TX+
- Pin 4: TX-
- Pin 5: RX+
- Pin 6: RX-
- Pin 7: GND
- Pin 8: TX+
- Pin 9: TX-
- Pin 10: RX+
- Pin 11: RX-
- Pin 12: GND
- Pin 13: TX+
- Pin 14: TX-
- Pin 15: RX+

**Wiring Details:**

- Pin 1 (SATA) is connected to Pin 1 (SATA III).
- Pin 2 (SATA) is connected to Pin 2 (SATA III).
- Pin 3 (SATA) is connected to Pin 3 (SATA III).
- Pin 4 (SATA) is connected to Pin 4 (SATA III).
- Pin 5 (SATA) is connected to Pin 5 (SATA III).
- Pin 6 (SATA) is connected to Pin 6 (SATA III).
- Pin 7 (SATA) is connected to Pin 7 (SATA III).
- Pin 8 (SATA) is connected to Pin 8 (SATA III).
- Pin 9 (SATA) is connected to Pin 9 (SATA III).
- Pin 10 (SATA) is connected to Pin 10 (SATA III).
- Pin 11 (SATA) is connected to Pin 11 (SATA III).
- Pin 12 (SATA) is connected to Pin 12 (SATA III).
- Pin 13 (SATA) is connected to Pin 13 (SATA III).
- Pin 14 (SATA) is connected to Pin 14 (SATA III).
- Pin 15 (SATA) is connected to Pin 15 (SATA III).

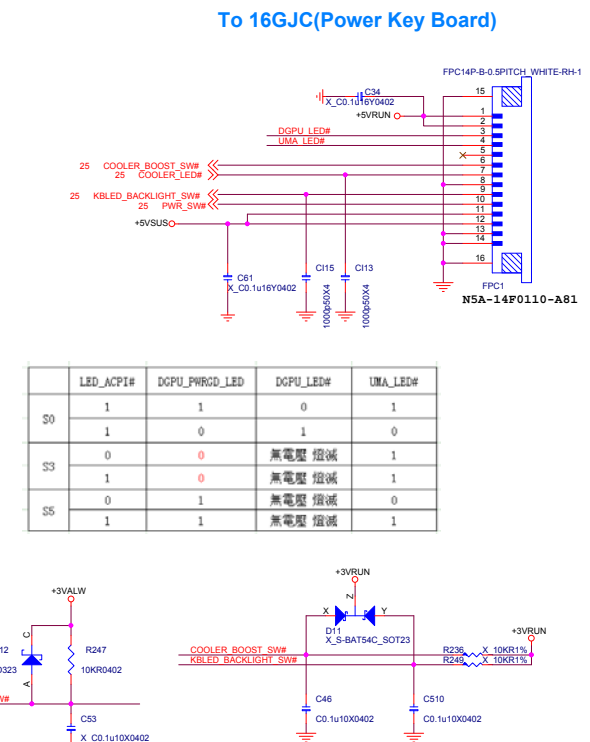
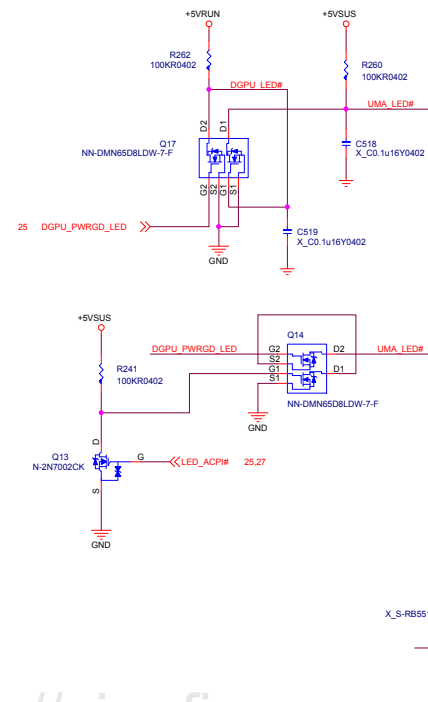
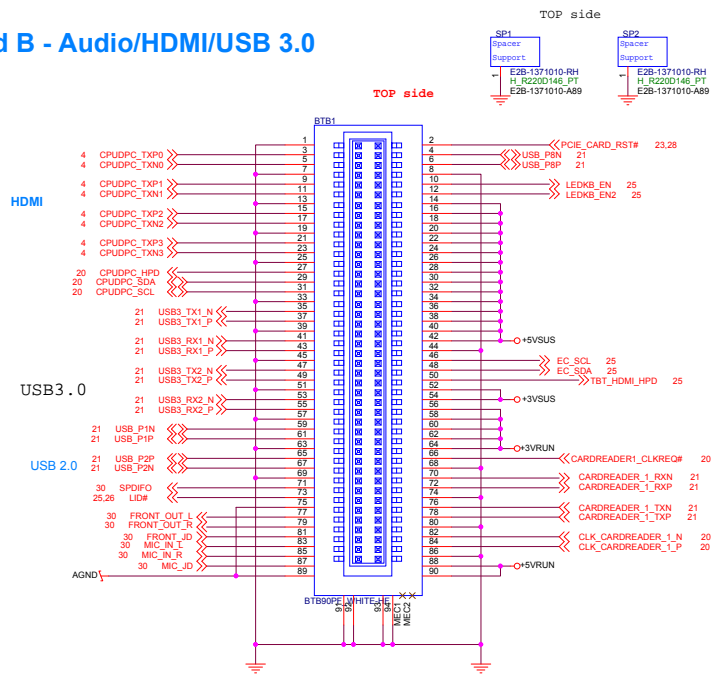
**Additional Components:**

- C615: 10uF 3.3V
- C616: 100nF 5V
- CON3: 3-pin connector
- MEC1: 1-pin connector
- MEC2: 1-pin connector

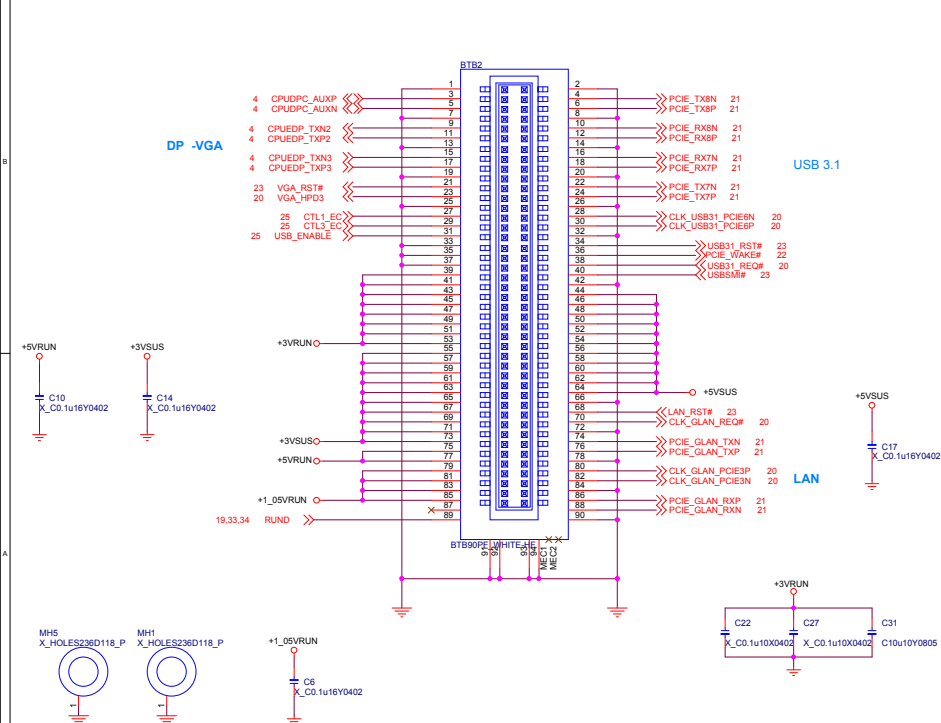
**Notes:**

- SATA22PSF BLACK-HF
- N9V-13F005-A81
- SATA\_13\_5

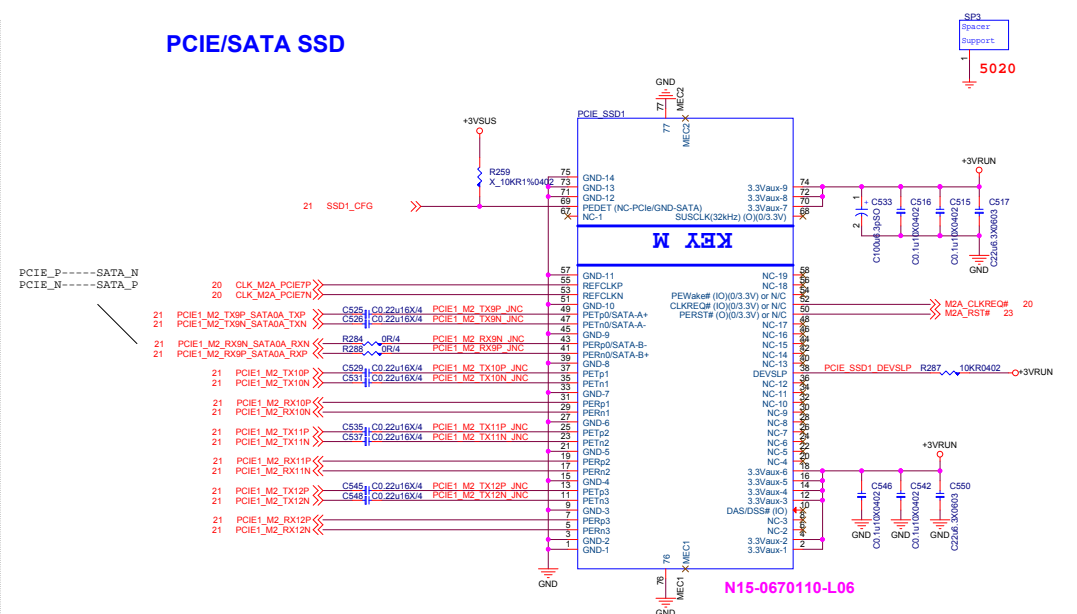
## Board B - Audio/HDMI/USB 3.0



## Board A - CRT/USB3.1/USB2.0/LAN



## PCIE/SATA SSD

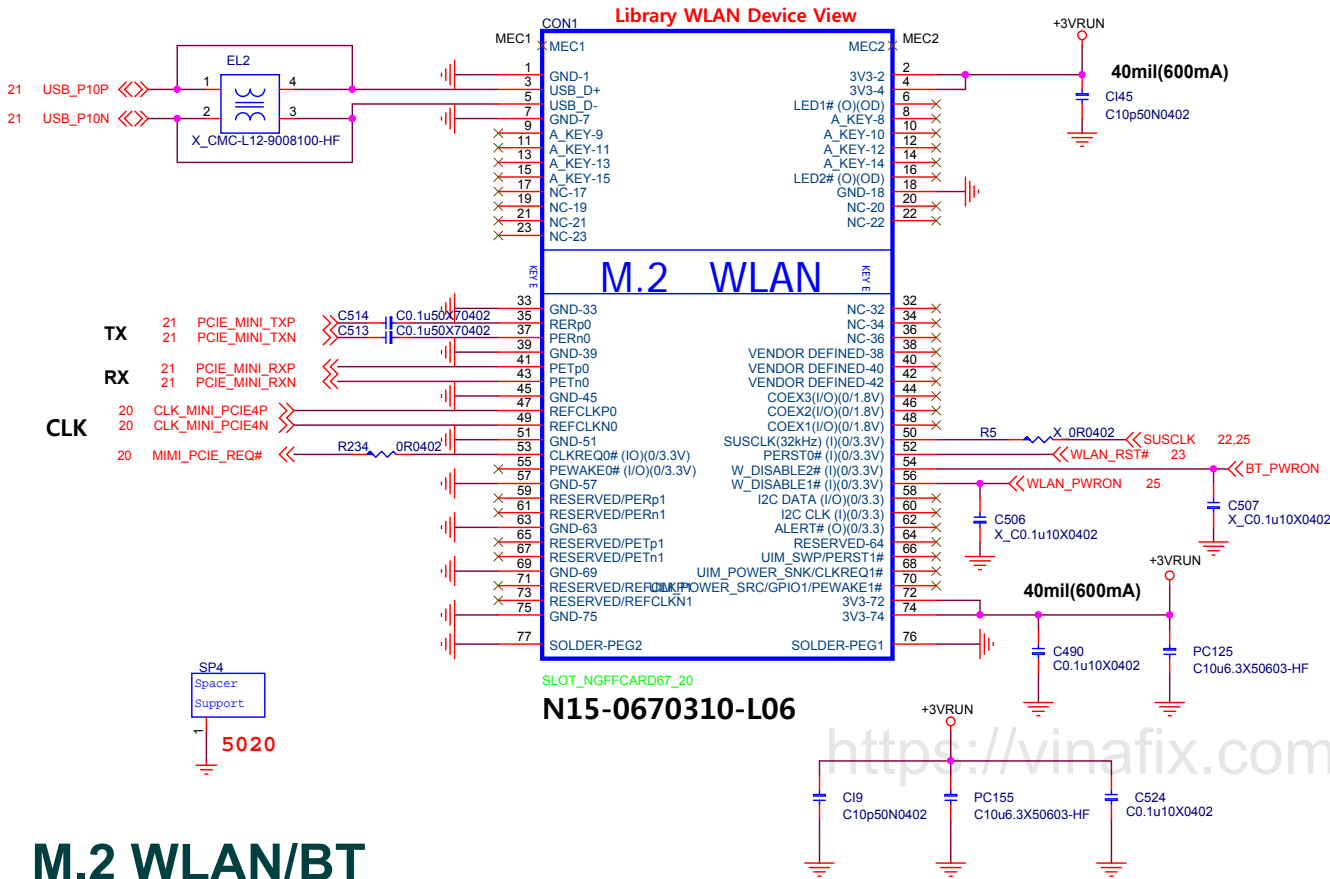


Condition	PCI Express® Gen 2 Only	PCI Express® Gen 3 Only	SATA Only	PCI Express® Gen 2/ SATA	PCI Express® Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF <sup>2</sup>	None	None <sup>3</sup>

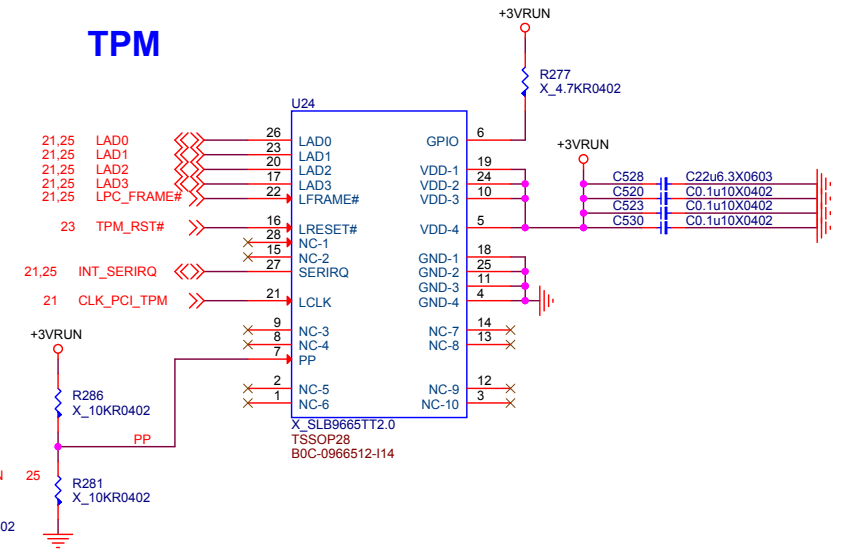




## Library WLAN Device View

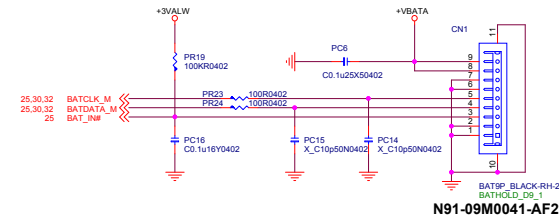


## TPM

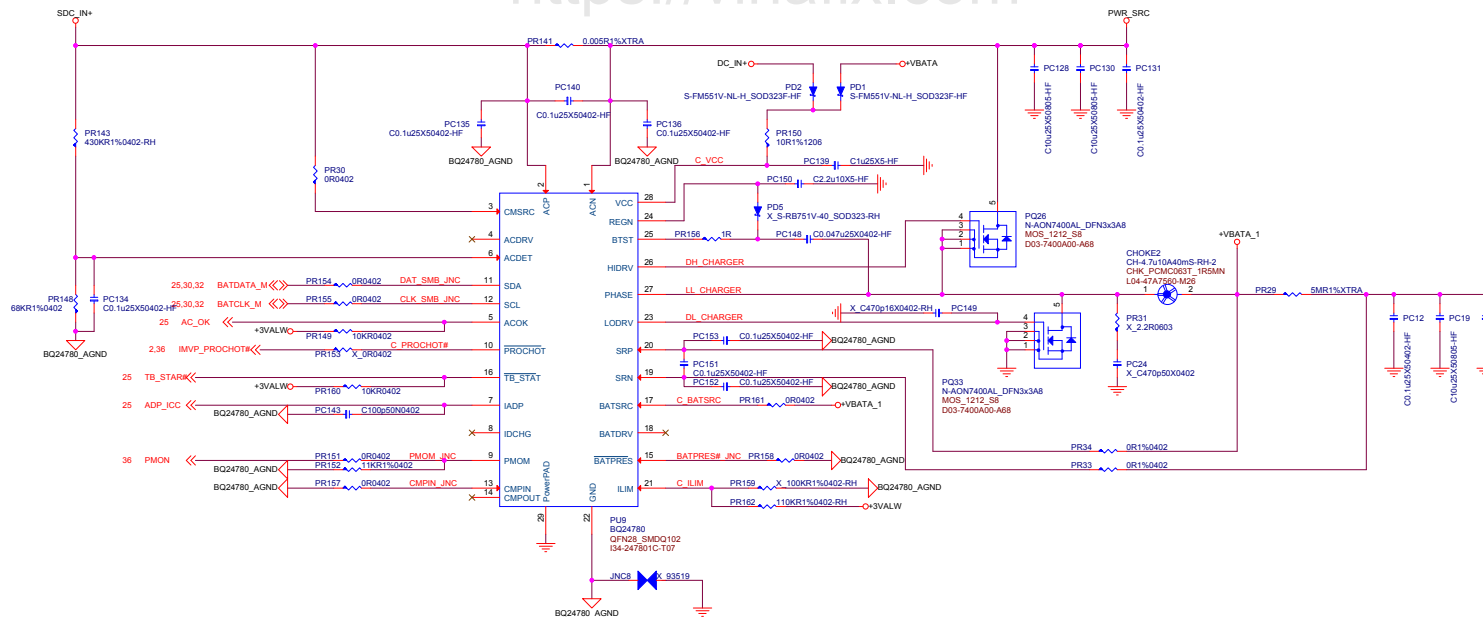


M.2 WLAN/BT

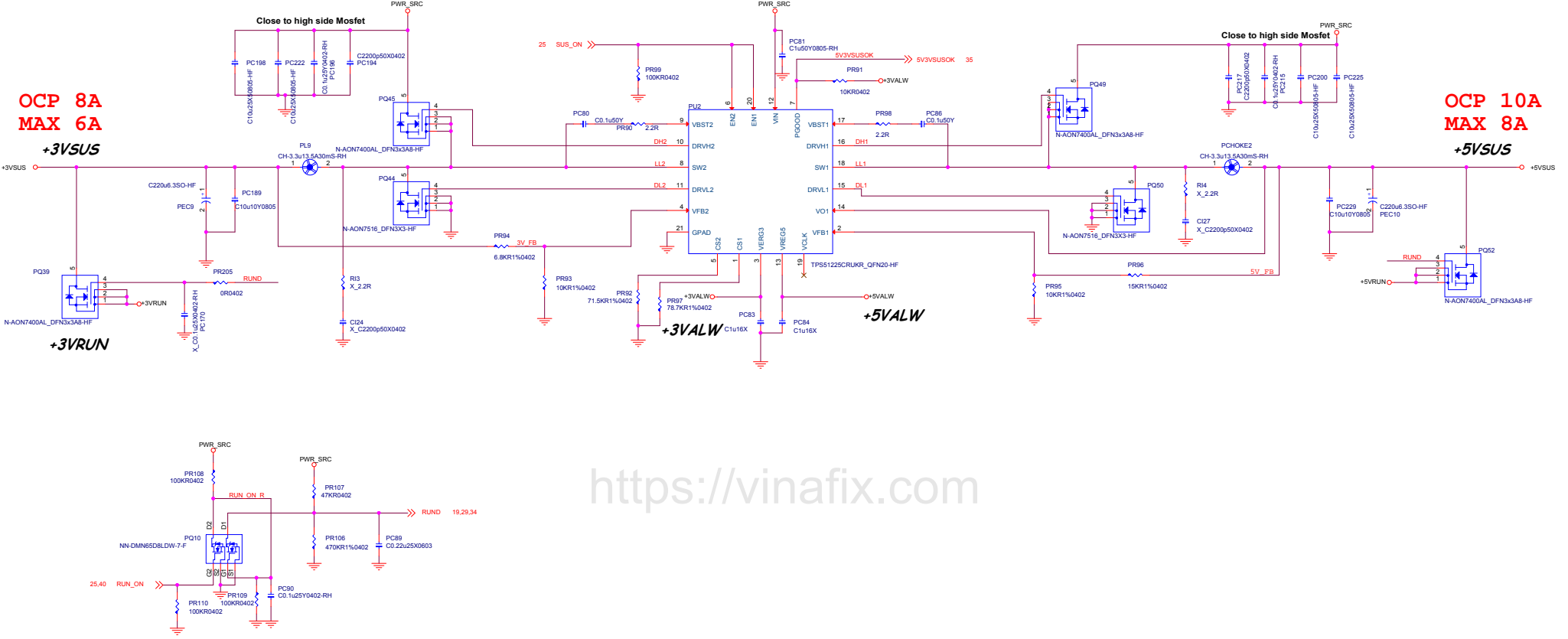
msi MICRO-STAR INT'L CO.,LTD.		
Title		
WLAN/TPM		
Size	Document Number	Rev
	MS-16GJ	10
Date:		Sheet 31 of 56



1: GND  
2: GND  
3: BAT\_IN#  
4: SMBDATA  
5: SMBCLK  
6: NC  
7: NC  
8: VBATA+  
9: VBATA+



# System Power



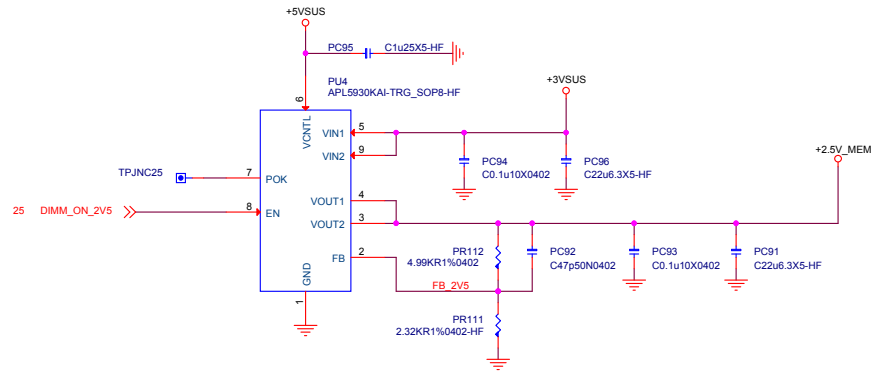
<https://vinafix.com>

Title		System Power	
Size	Custom	Document Number	Rev 10
MS-16GJ		Date: Wednesday, July 29, 2015	
Sheet		33 of 56	



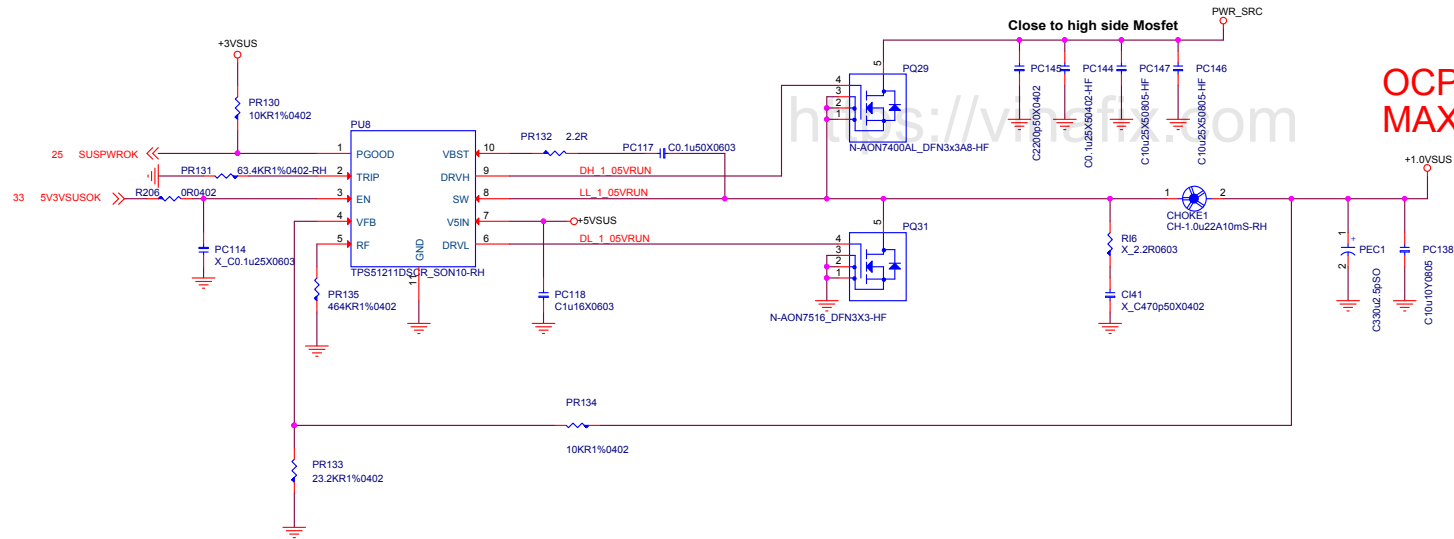
## +2.5V\_MEM

OCP 4.2A  
MAX 1A



## +1.0VSUS

OCP 10A  
MAX 8A



Skylake H-line 42e 45W ISL95855

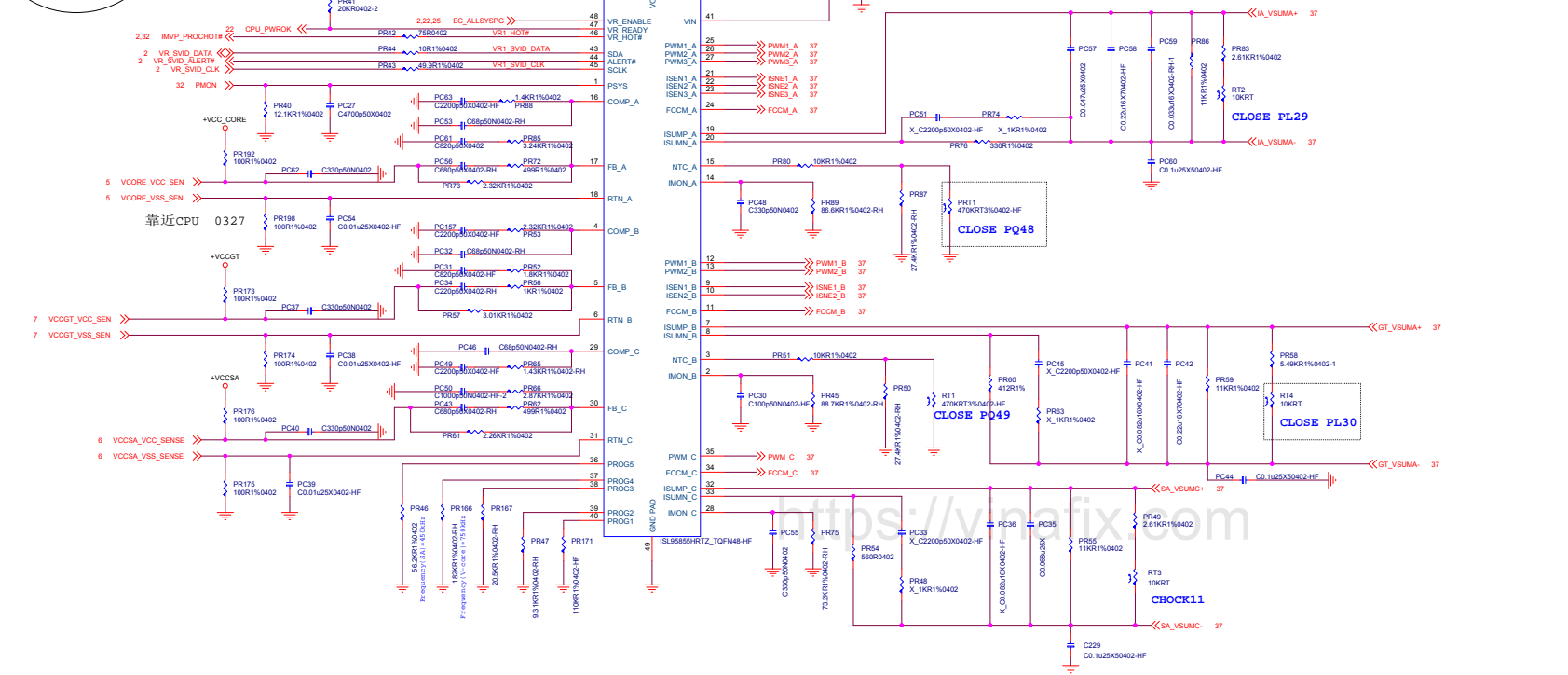
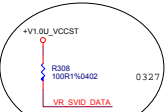


TABLE 4. PROG1 PROGRAMMING TABLE

TYPICAL PROG1 RESISTOR (±1%, kΩ)	VR A + VR B + VR C (Ω/US)	BLEW BLAT ALL VRs (mm/μs)	ADDRESS SELECTION	VR A	VR B	VR C
1.87	1.05	30	6T[01A]	GTUS [03H]	6A [02H]	
5.62	1.05	30	6T[01A]	IA [00H]	GTUS [03H]	
9.31	1.05	30	6T[01A]	IA [00H]	6A [02H]	
13.9	1.05	30	IA [00H]	GTUS [03H]	6A [02H]	
16.9	1.05	30	IA [00H]	6T[01A]	GTUS [03H]	
20.5	1.05	30	IA [00H]	6T[01A]	6A [02H]	
24.3	1.05	10	6T[01A]	GTUS [03H]	6A [02H]	
28.0	1.05	10	6T[01A]	IA [00H]	GTUS [03H]	
34.0	1.05	10	6T[01A]	IA [00H]	6A [02H]	
41.2	1.05	10	IA [00H]	GTUS [03H]	6A [02H]	
48.7	1.05	10	IA [00H]	6T[01A]	GTUS [03H]	
56.2	1.05	10	IA [00H]	6T[01A]	6A [02H]	
63.4	0	30	6T[01A]	GTUS [03H]	6A [02H]	
71.5	0	30	6T[01A]	IA [00H]	GTUS [03H]	
78.7	0	30	6T[01A]	IA [00H]	6A [02H]	
88.7	0	30	IA [00H]	GTUS [03H]	6A [02H]	
100	0	30	IA [00H]	6T[01A]	GTUS [03H]	
110	0	30	IA [00H]	6T[01A]	6A [02H]	
121	0	10	6T[01A]	GTUS [03H]	6A [02H]	
137	0	10	6T[01A]	IA [00H]	GTUS [03H]	
150	0	10	6T[01A]	IA [00H]	6A [02H]	
165	0	10	IA [00H]	GTUS [03H]	6A [02H]	
182	0	10	IA [00H]	6T[01A]	GTUS [03H]	
215	0	10	IA [00H]	6T[01A]	6A [02H]	

TYPICAL PROG2 PROGRAMMING TABLE				
TYPICAL PROG2 RESISTOR (±1%, kΩ)	IMAX VR A			VR A P81L P81L REDUCTION
	3-PH(A)	2-PH(A)	1-PH(A)	
1.87	67	35	7	2-Phase
5.62	70	40	10	2-Phase
9.31	75	45	15	2-Phase
13.9	80	50	18	2-Phase
16.9	85	55	20	2-Phase
20.5	91	60	25	2-Phase
24.3	95	65	27	2-Phase
28.0	100	67	30	2-Phase
34.0	105	70	33	2-Phase
41.2	110	75	35	2-Phase
48.7	115	80	40	2-Phase
56.2	120	85	45	2-Phase
63.4	67	35	7	1-Phase
71.5	70	40	10	1-Phase
78.7	75	45	15	1-Phase
88.7	80	50	18	1-Phase
100	85	55	20	1-Phase
110	91	60	25	1-Phase
121	95	65	27	1-Phase
137	100	67	30	1-Phase
150	105	70	33	1-Phase
165	110	75	35	1-Phase
182	115	80	40	1-Phase
215	120	85	45	1-Phase

TABLE 6. PROG3 PROGRAMMING TABLE				
TYPICAL PROG3 RESISTOR (±1%, kΩ)	IMAX VR B		DROOP VR B	
	2PH (A)	1PH (A)		
1.87	35	7	Active	
5.62	40	10	Active	
9.31	45	15	Active	
13.9	50	18	Active	
16.9	55	20	Active	
20.5	60	25	Active	
24.3	65	27	Active	
28.0	67	30	Active	
34.0	70	33	Active	
41.2	75	35	Active	
48.7	80	40	Active	
56.2	85	45	Active	
63.4	35	7	Disabled	
71.5	40	10	Disabled	
78.7	45	15	Disabled	
88.7	50	18	Disabled	
100	55	20	Disabled	
110	60	25	Disabled	
121	65	27	Disabled	
137	67	30	Disabled	
150	70	33	Disabled	
165	75	35	Disabled	
182	80	40	Disabled	
215	85	45	Disabled	

TABLE 7. PROG4 PROGRAMMING TABLE

TYPICAL PROG4 RESISTOR (±1%, kΩ)	DROOP VR A	DROOP VR C	VR A and VR B SWITCHING FREQUENCY (kHz)
1.87	Disabled	Disabled	300
5.62	Disabled	Disabled	350
9.31	Disabled	Disabled	450
13.9	Disabled	Disabled	583
16.9	Disabled	Disabled	750
20.5	Disabled	Disabled	1000
24.3	Disabled	Active	300
28.0	Disabled	Active	350
34.0	Disabled	Active	450
41.2	Disabled	Active	583
48.7	Disabled	Active	750
56.2	Disabled	Active	1000
63.4	Active	Disabled	300
71.5	Active	Disabled	350
78.7	Active	Disabled	450
88.7	Active	Disabled	583
100	Active	Disabled	750
110	Active	Disabled	1000
121	Active	Active	300
137	Active	Active	350
150	Active	Active	450
165	Active	Active	583
182	Active	Active	750
215	Active	Active	1000

TABLE 8. PROG5 PIN

TYPICAL PROG5 RESISTOR (±1%, kΩ)	VR C IMAX (A)	VR C SWITCHING FREQUENCY (kHz)	
1.87	7	17	300
5.62	9	20	300
9.31	12	25	300
13.9	15	27	300
16.9	7	17	350
20.5	9	20	350
24.3	12	25	350
28.0	15	27	350
34.0	7	17	450
41.2	9	20	450
48.7	12	25	450
56.2	15	27	450
63.4	7	17	583
71.5	9	20	583
78.7	12	25	583
88.7	15	27	583
100	7	17	750
110	9	20	750
121	12	25	750
137	15	27	750
150	7	17	1000
165	9	20	1000
182	12	25	1000
215	15	27	1000

EVT: power change list (H4+2)

CPU-core

PR157 32.2R (0603 R11-022A013-W08)

PR613 32.43K (R11-2431T12-W08)

PC159 1000P (C11-1027612-W08)

PR608 34.7K (R11-0472T12-W08)

PR615 385.6K (R11-8662T12-W08)

PC194 30.22uF (C11-2242312-W08)

PC193 347nF (C11-4732012-W08)

Aux PC288 10nF (C11-1032052-T34)

EVT: power change list (H4+2)

GT-core

PR607 3383R (0603 PN-R11-3830T13-W08)

PR622 32.54K (R11-2941T12-W08)

PC27 8500P (C11-851822-T01)

PR664 31.4K (R11-0142T12-W08)

PC287 3200P (C11-2217812-W08)

PR663 3.1K (R11-0102T12-W08)

PR671 386.6K (R11-8662T12-W08)

PC234 1000P (C11-1012812-W08)

PC232 30.22uF (C11-2242312-T04)

PR668 35.49K (R11-5491T12-W08)

EVT: power change list (H4+2)

SA-core

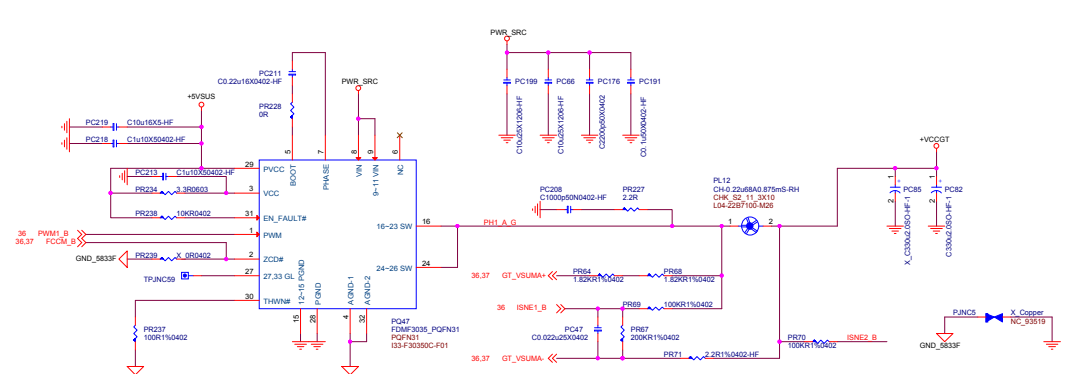
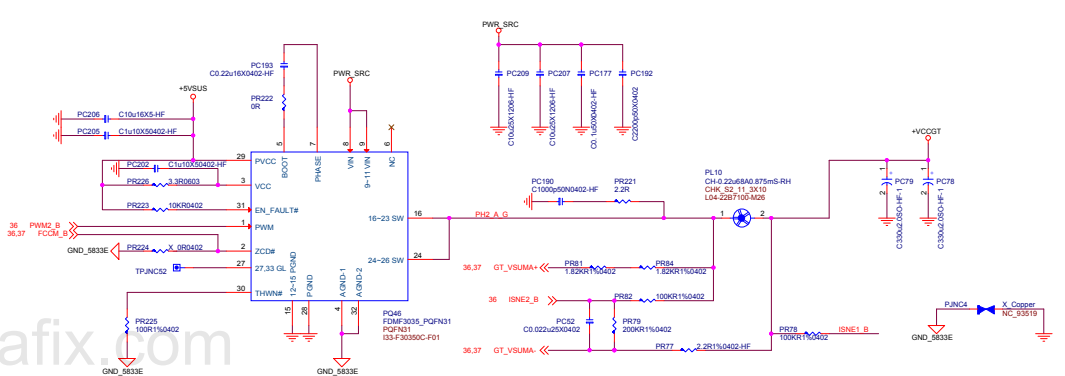
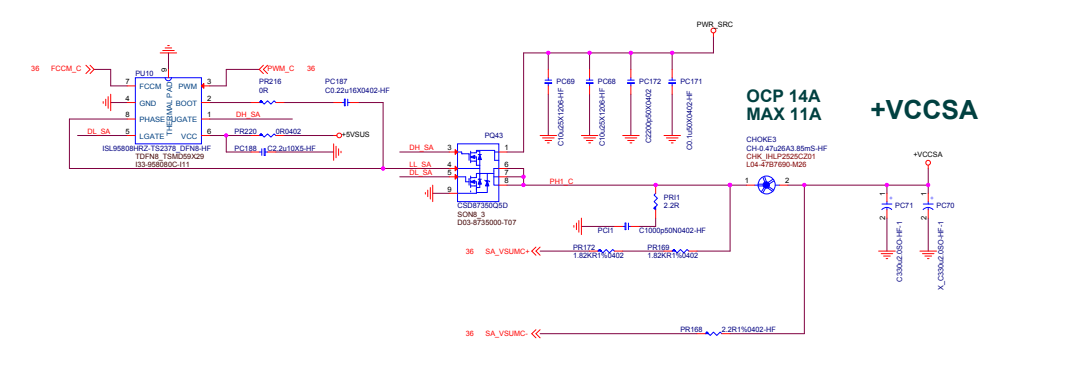
PR62132.26K (R11-2261T12-W08)

PC20731.2nF (C11-1222832-W08)

PR61832.87K (R11-2871T12-W08)

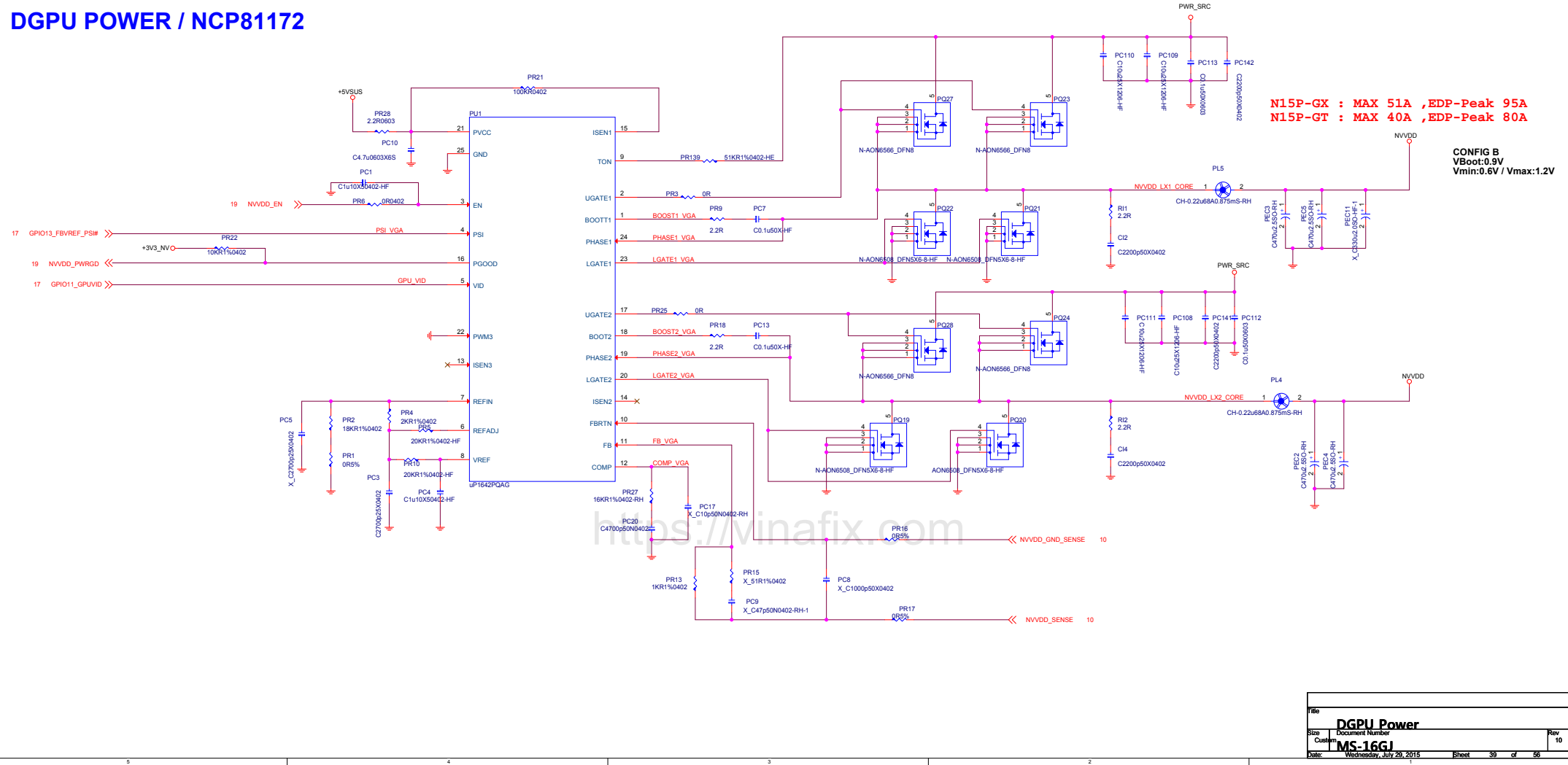
PR626371.5K (R11-7152T22-W08)





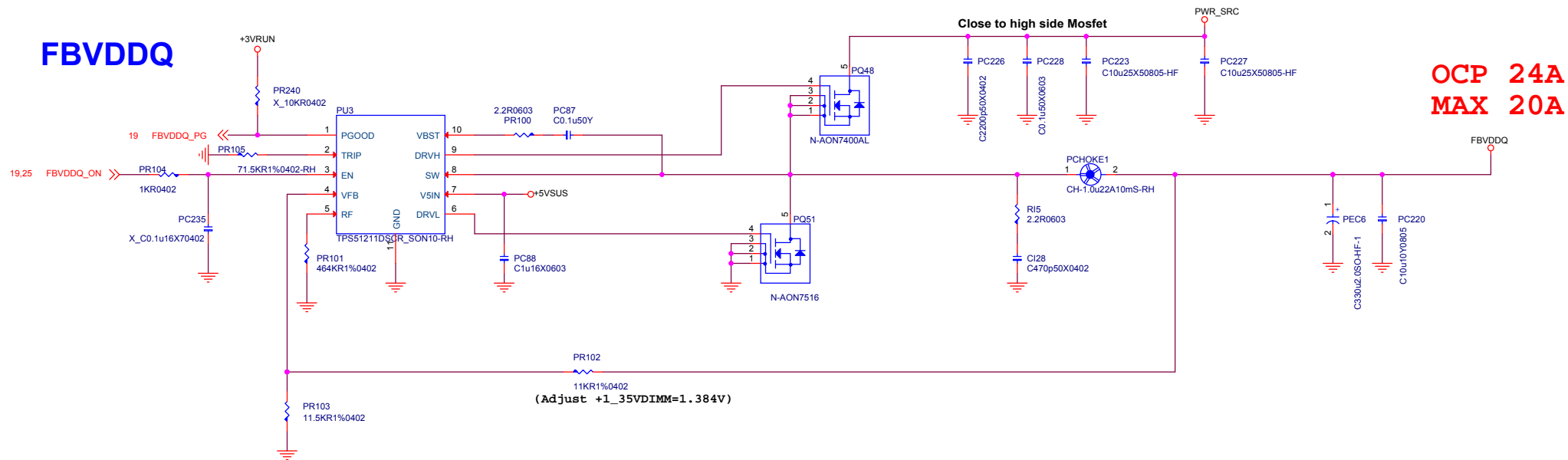


# DGPU POWER / NCP81172



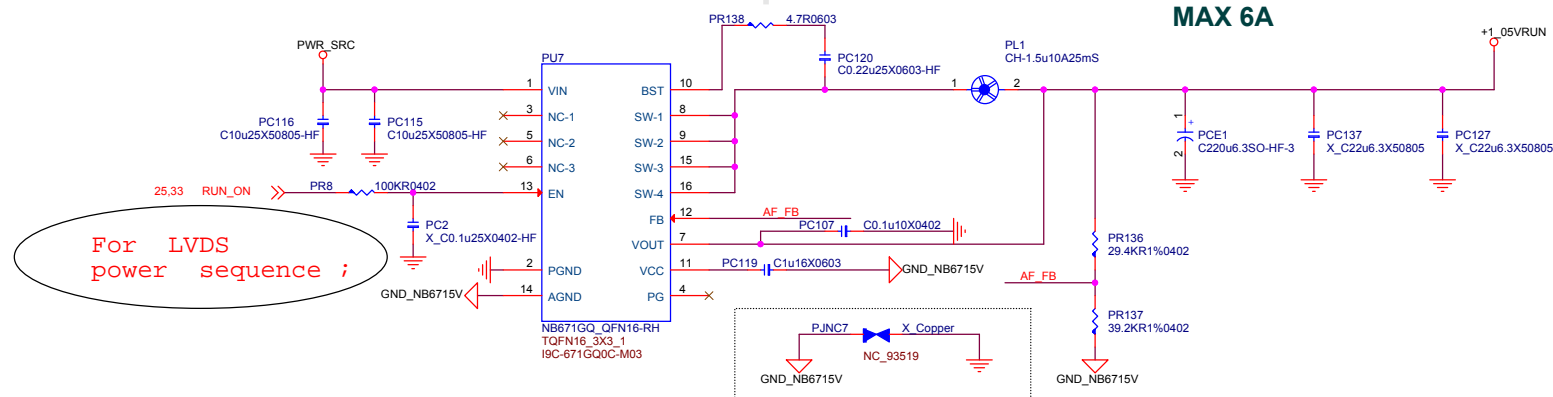
File	DGPU Power	Rev	10
Size	Document Number	Sheet	39 of 56
Custom	MS-16GJ	Date	Wednesday, July 28, 2015

FBVDDQ



<https://vinafix.com>

OCP 8A  
MAX 6A

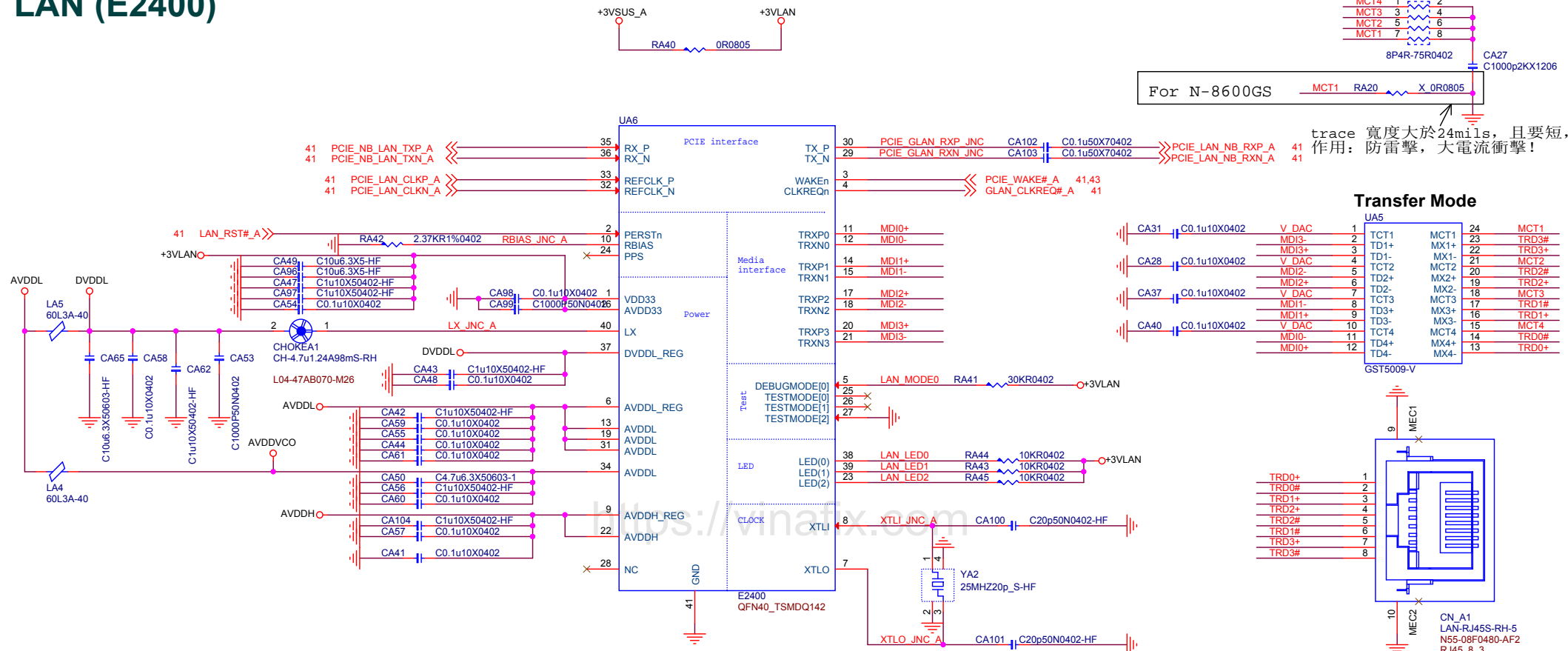


For LVDS  
power sequence ;

Title		
+1_35VDIMM/+0_675VRUN		
Size	Document Number	Rev
Custom	MS-16GJ	10
Date:	Friday, July 31, 2015	Sheet 40 of 56



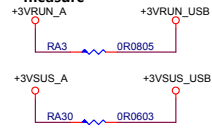
## LAN (E2400)



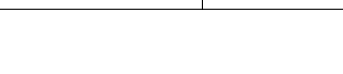
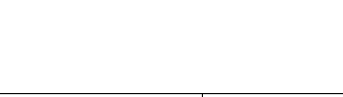
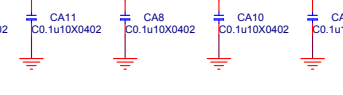
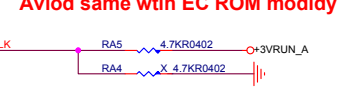
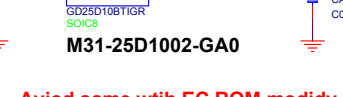
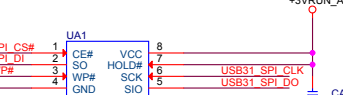
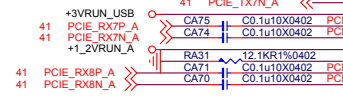
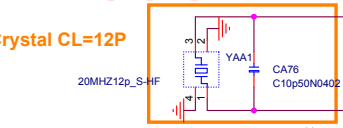
Title			
[A] GIGA LAN(BFN2205B)			
Size	Document Number	Rev	
Custom	MS-16GJ	10	
Date:	Wednesday, July 29, 2015	Sheet	42 of 56

# PCIE to USB 3.1

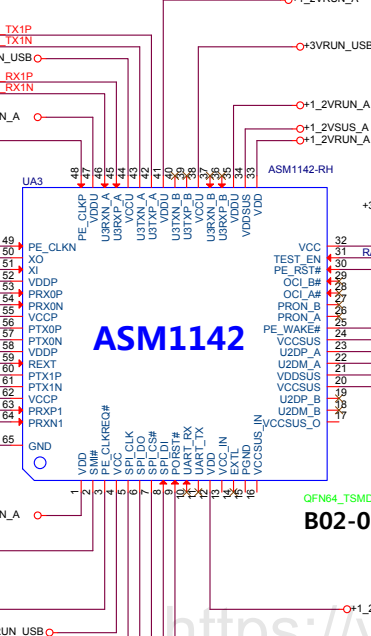
## For 0A Consumption measure



## PCB 1.1 3Crystal CL=12P

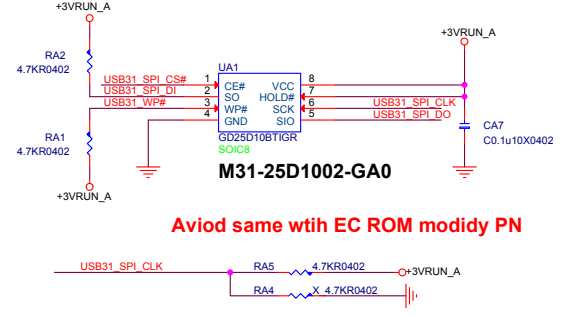


## ASM1142



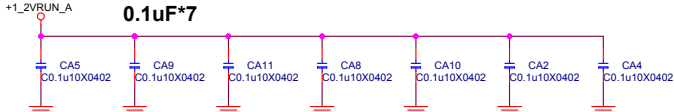
B02-011422C-AD0

## SPI ROM For FW ( stuff first)

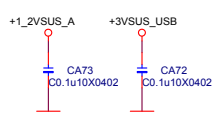


Aviod same with EC ROM modidy PN

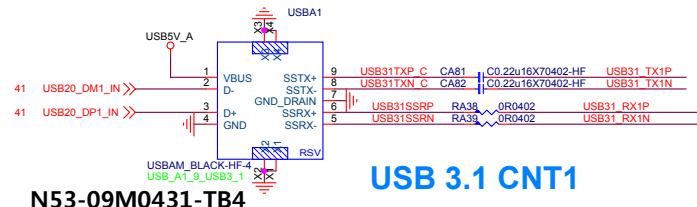
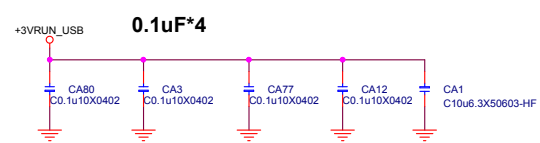
0.1uF\*7



0.1uF\*2



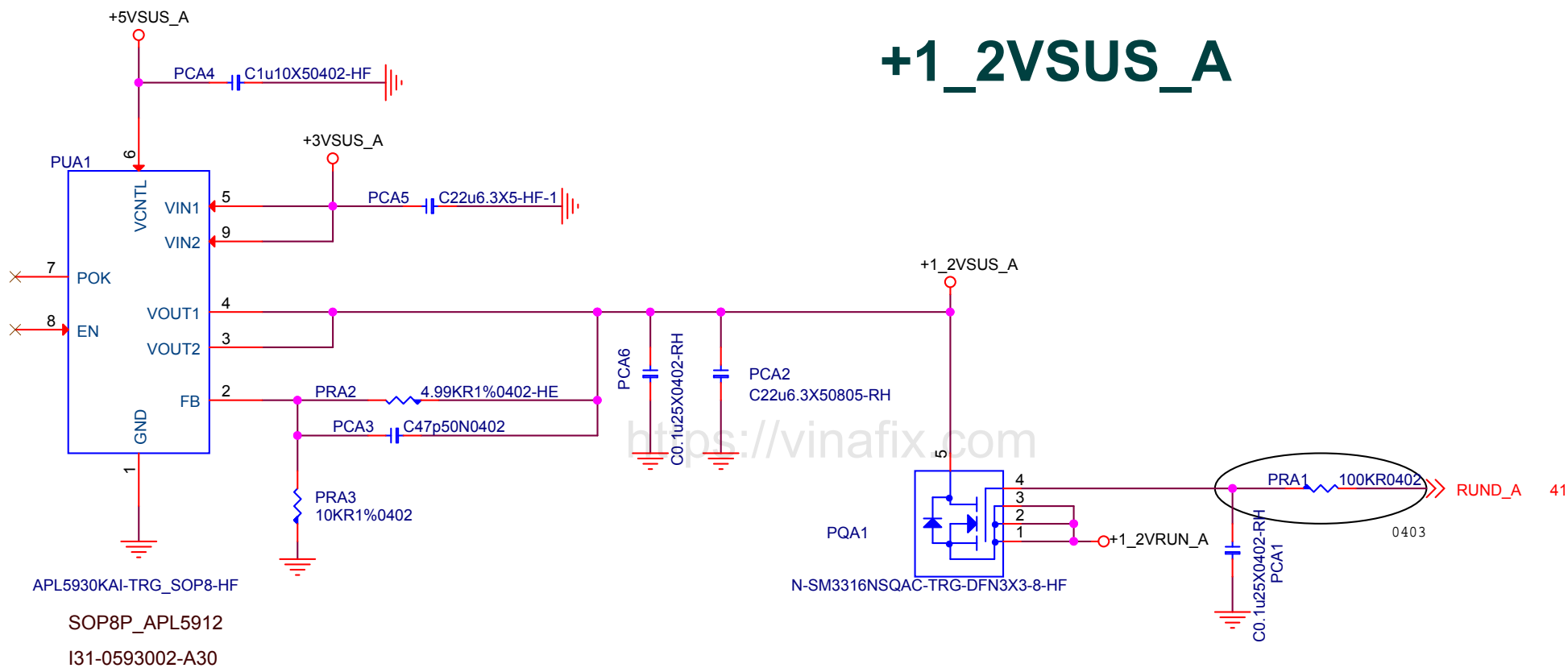
0.1uF\*4



USB 3.1 CNT1

N53-09M0431-TB4

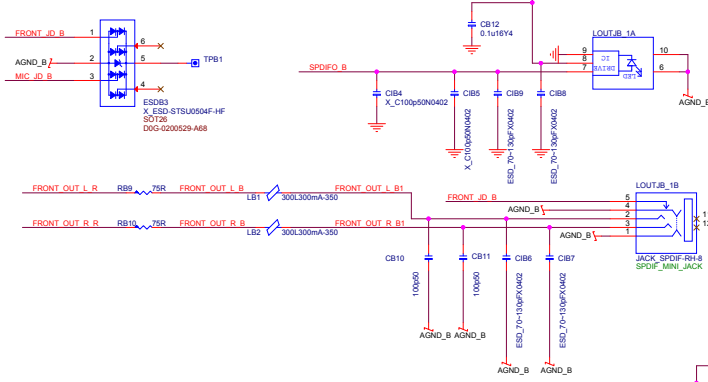
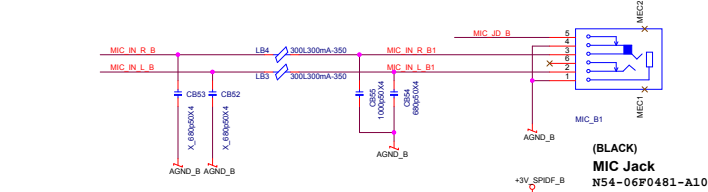
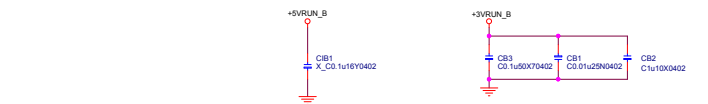
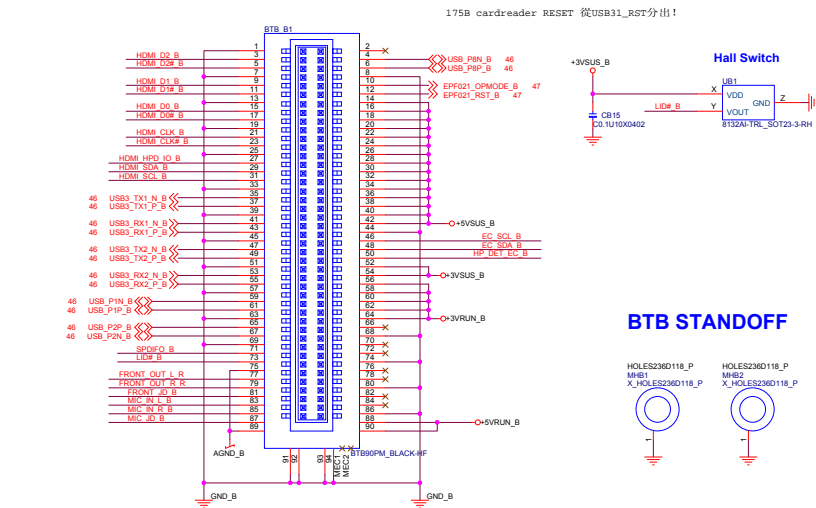
Title		[B] USB3.0x2/USB2.0x1/LED KB	
Size	Custom	Document Number	MS-16GJ
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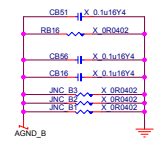
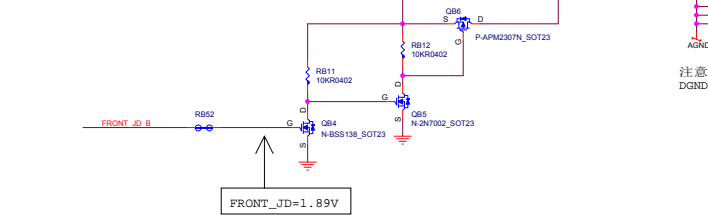
Title			
<b>+1_2VSUS_A/+1_2VRUN_A</b>			
Size A	Document Number <b>MS-16GJ</b>		Rev 10
Date:	Friday, July 31, 2015	Sheet	44 of 56



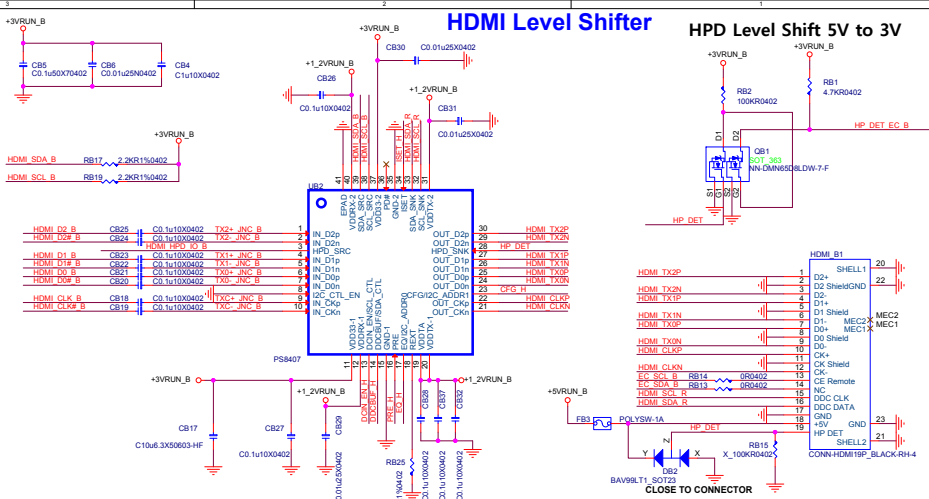
## 16GCB board to board CONN1: HDMI,Audio, LED,LID



**Power** QB27 VGS\_ON : -1V~-2V

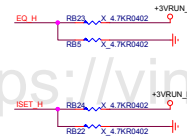


注意預防noise 串到DGND,  
DGND再串到AGND----0402



3 Level Input:  
L: LOW, internal pull down  
H: HIGH, external pull up  
M: VDD33/2, both external pull-up and pull-down

```
Configuration pin, 3.3V IO, internal pull down
at ~150k Ohm. 3.3V I/O.
L: HDMI ID disable
H: HDMI ID enable
```



```
Receiver equalization setting; Internal pull down at
~150k Ohm, 3.3V I/O.
L: programmable EQ for channel loss up to 12.4dB
H: programmable EQ for channel loss up to 4.3dB
M: programmable EQ for channel loss up to 8.6dB
```

```

TMD5 output swing adjustment; Internal pull down at ~150
Ohm, 3.3V I/O.
  L: default
  H: increase +13%
  M: reduce -13%

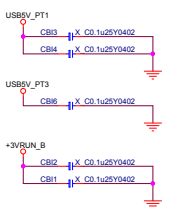
```

DC coupling enable; Internal pull down at ~150k Ohm  
3.3V I/O.  
L: default, AC coupling input  
H: DC coupling input

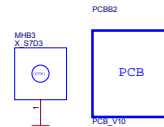
```
Enable active DDC buffer/ Internal pull down at -150K Ohm,
3.3V I/O
L: default, passive DDC pass-through
H: active DDC buffer with default threshold
M: active DDC buffer without internal pull up resistor
```

Output pre-emphasis setting; Internal pull down at ~150k Ohm, 3.3V I/O.

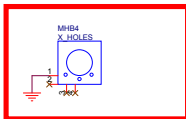
- L: no pre-emphasis
- H: 1.6dB pre-emphasis
- M: 2.5dB pre-emphasis



**EMI Cap**

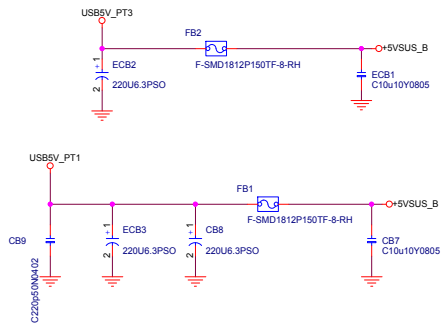


**SCREW HOLE**

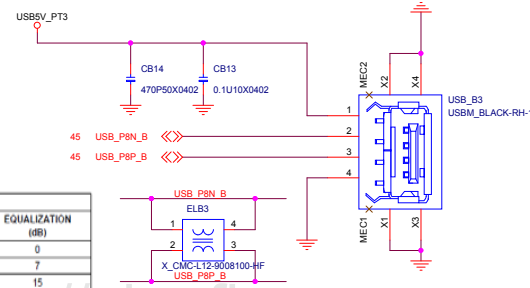


File: **[B] BTB CNT/Audio/HDMI**  
 Size: Occurrence Number  
 Custom: **MS-16GJ** Rev 10  
 Date: Tuesday, August 04, 2015 Sheet 45 of 56

**(USB3.0 Left Side - UP)**

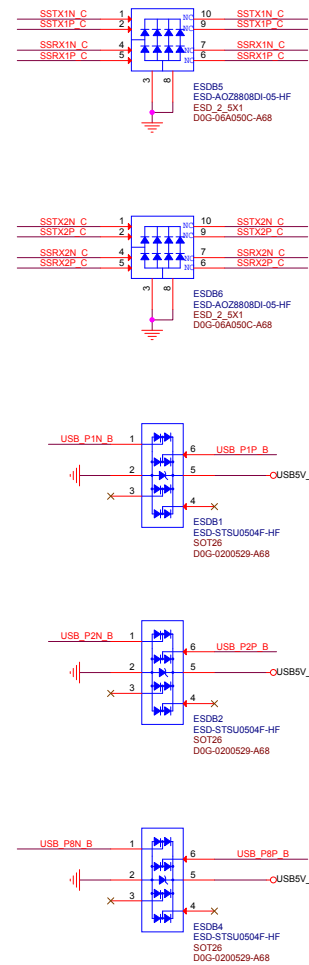


## USB 3.0 CNT 2



OUTPUT SWING AND EQ CONTROL (at 2.5 GHz)			
OSx <sup>(1)</sup>	TRANSISTION BIT AMPLITUDE (TYP mVpp)	Eqx <sup>(1)</sup>	EQUALIZATION (dB)
NC (default)	1042	NC (default)	0
0	908	0	7
1	1127	1	15
OUTPUT DE CONTROL (at 2.5 GHz)			
	OSx <sup>(1)</sup> = NC	OSx <sup>(1)</sup> = 0	OSx <sup>(1)</sup> = 1
NC (default)	0 dB	0 dB	0 dB
0	-3.5 dB	-2.2 dB	-4.4 dB
1	-6.0 dB	-5.2 dB	-6.0 dB
CONTROL PINS SETTINGS			
EN_RXD	DEVICE FUNCTION		
1 (default)	Normal Operation		
0	Sleep Mode		

(USB3.0 Left Side - Down)

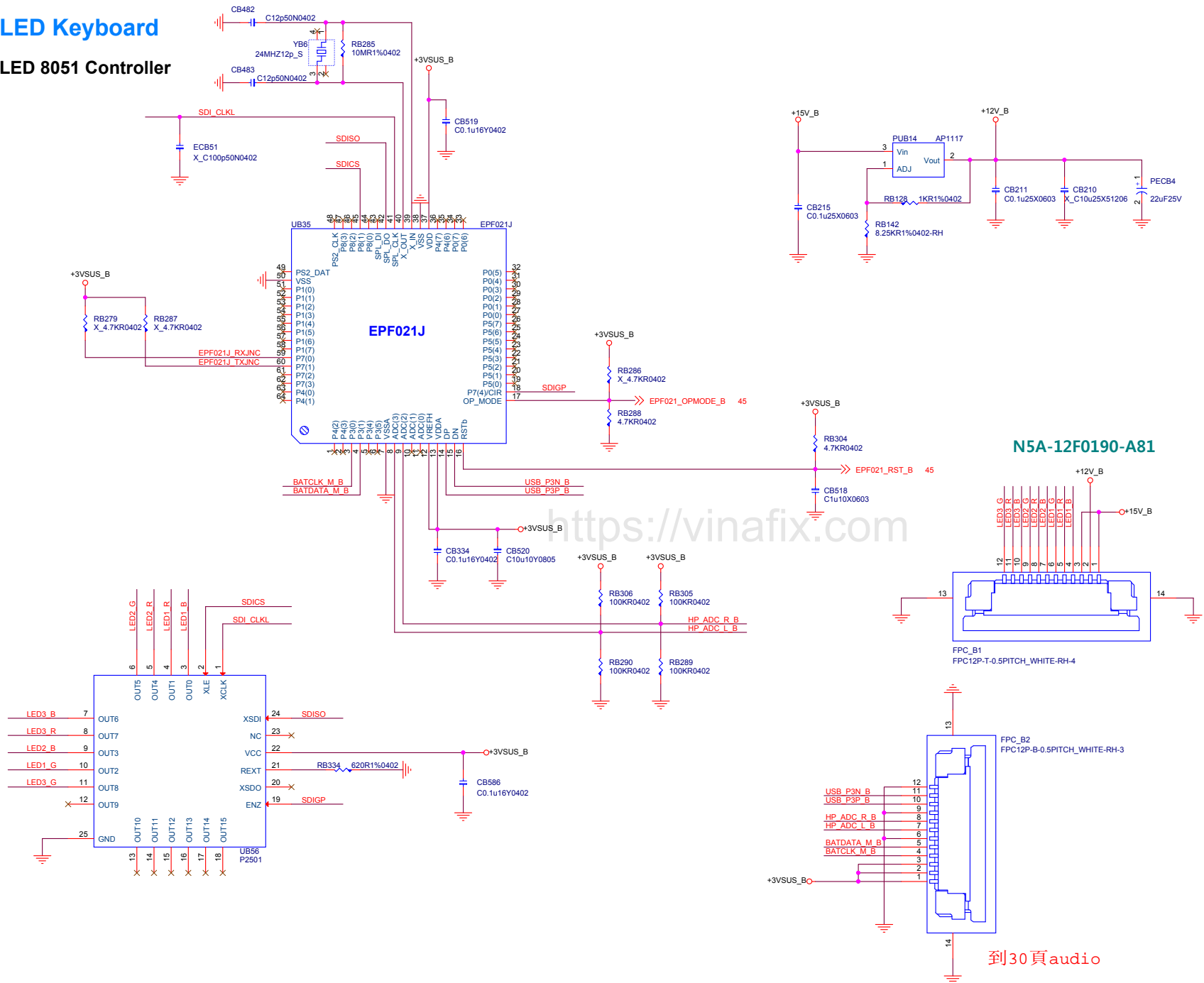


**[B] USB3.0x2/USB2.0x1**

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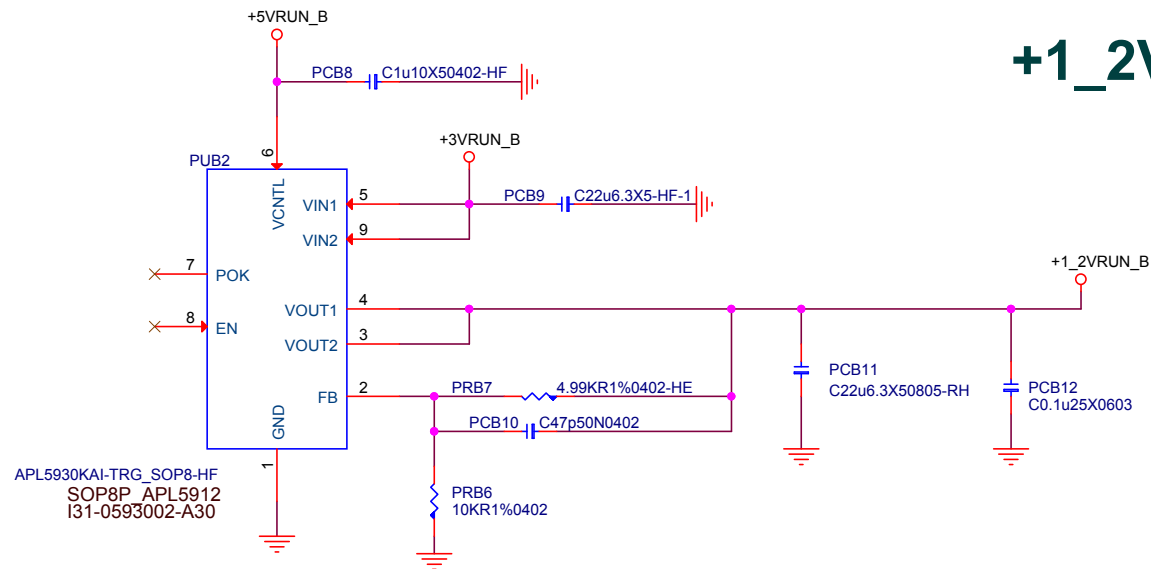
# LED Keyboard

## LED 8051 Controller



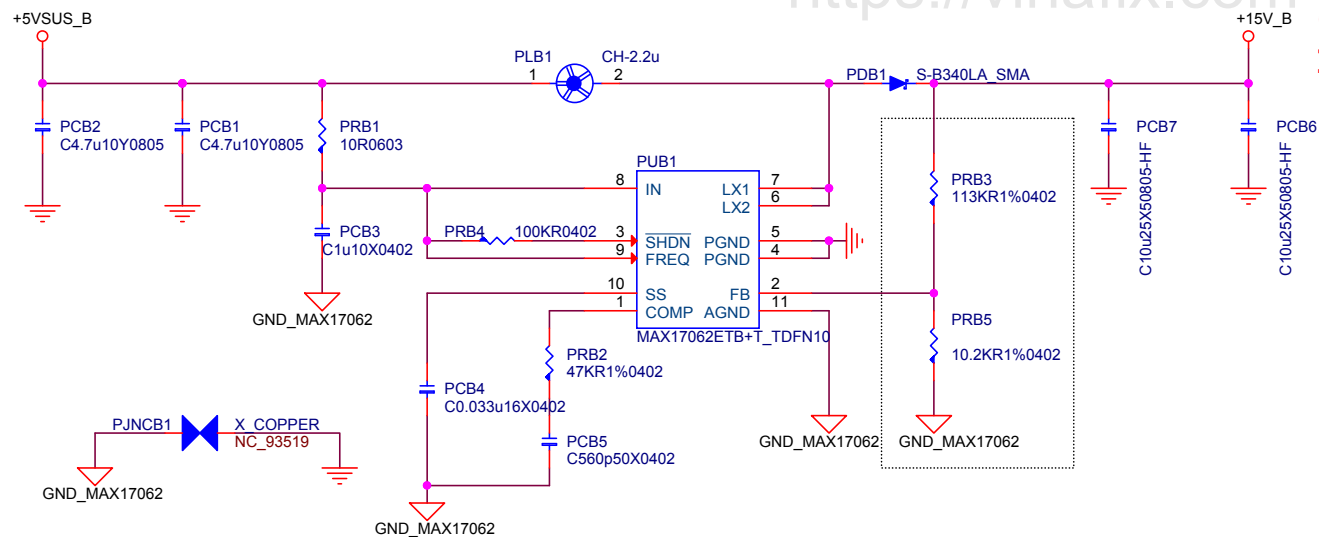
到30頁audio

Title		
[B] LED KB		
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Date:	Monday, August 03, 2015	Sheet 47 of 56



**+1\_2VRUN\_B**

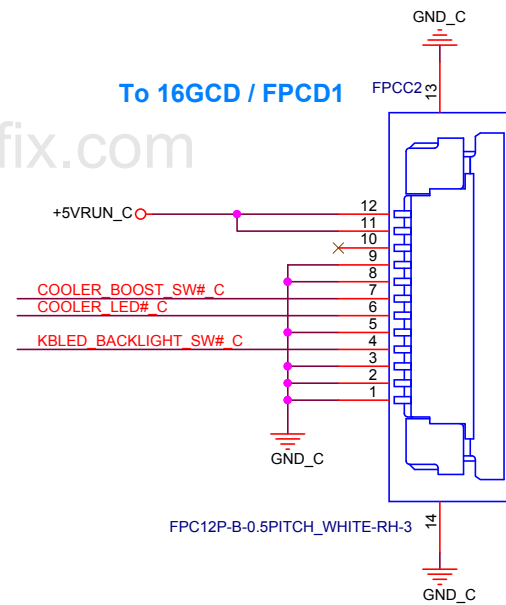
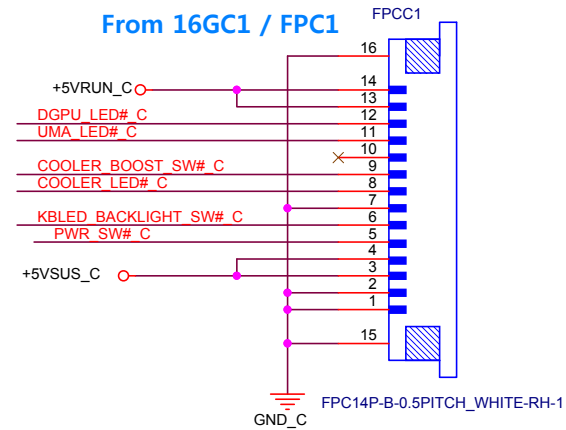
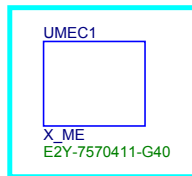
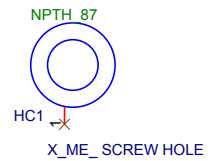
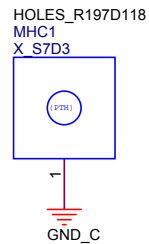
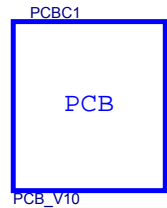
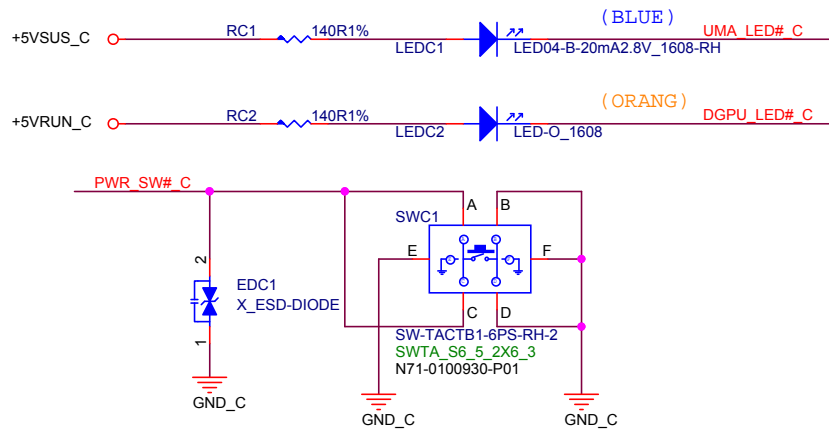
<https://vinafix.com>



**+15V**

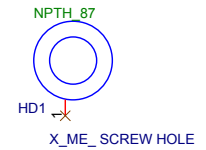
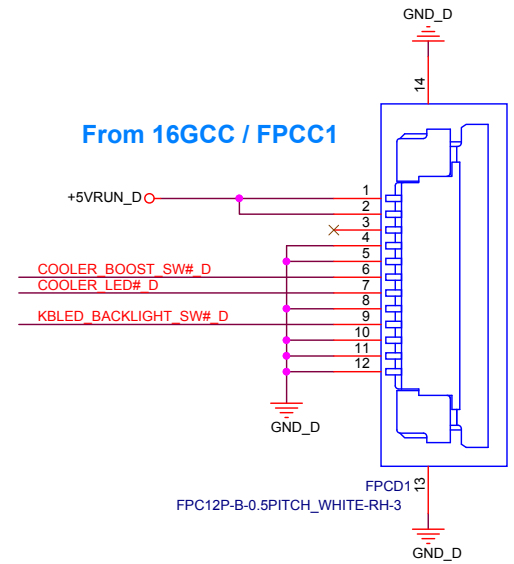
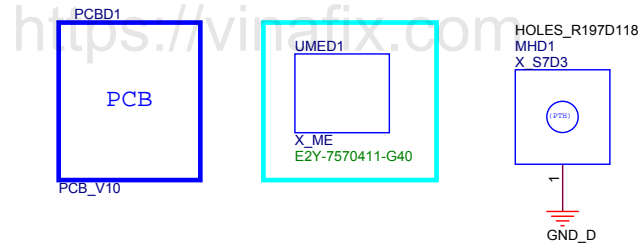
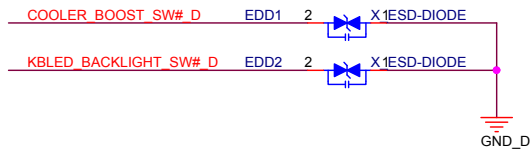
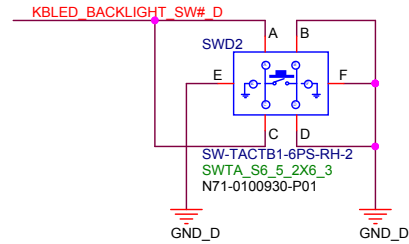
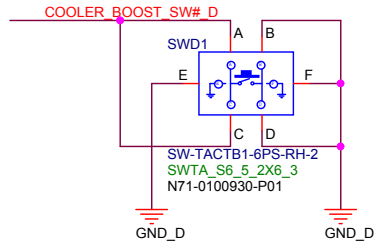
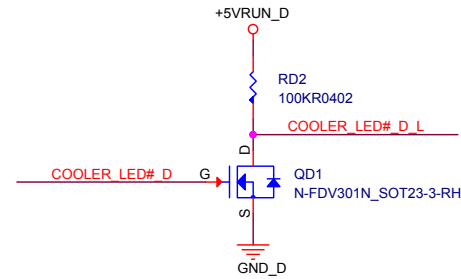
**OCP 0.6A**  
**MAX 0.5A**

Title			
<b>[B] +1_2VRUN_B /_15V_B</b>			
Size	Document Number		Rev
Custom	<b>MS-16GJ</b>		10
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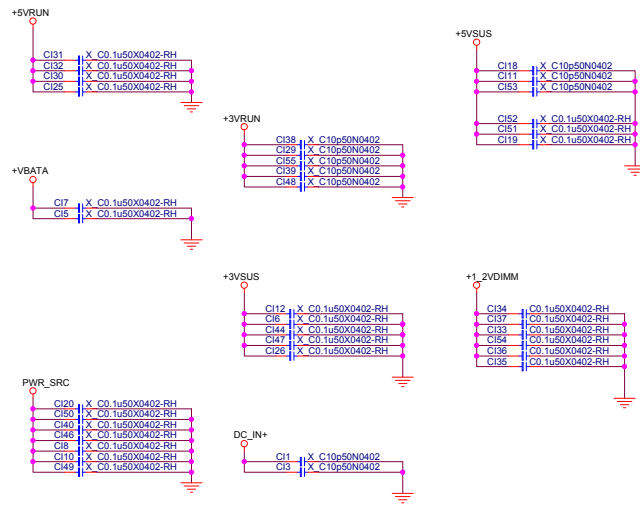


<https://vinafix.com>

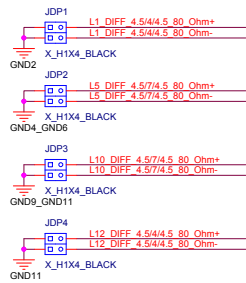
Title		
[C] Power SW Board		
Size	Document Number	Rev
Custom	MS-16GJ	10
Date:	Tuesday, August 04, 2015	Sheet 49 of 56



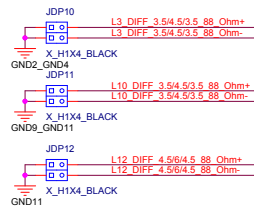
Title			
[D] Launch Board			
Size	Document Number	Rev	
Custom	MS-16GJ	10	
Date:	Tuesday, August 04, 2015	Sheet	50 of 56



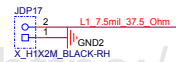
## 80 OHM



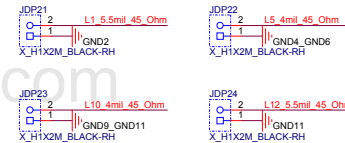
## 88 OHM



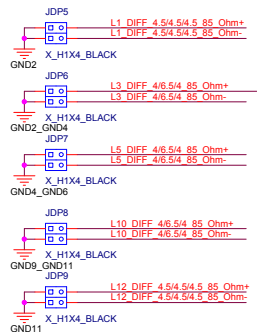
## 37.5 OHM



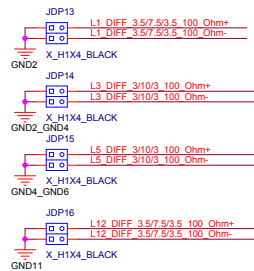
## 45 OHM



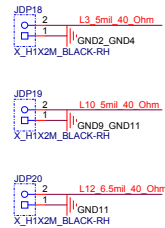
## 85 OHM



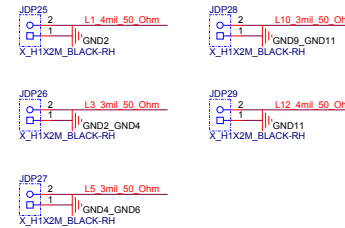
## 100 OHM

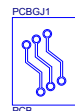
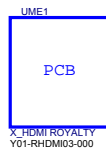
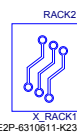
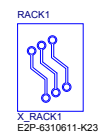
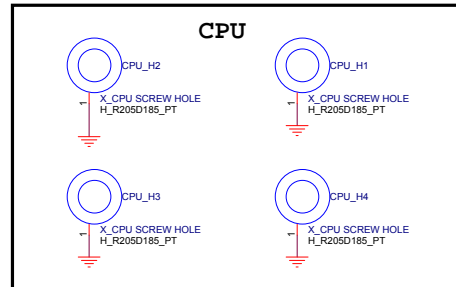
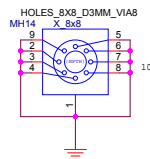
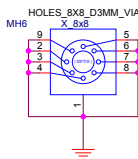
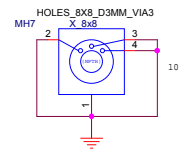
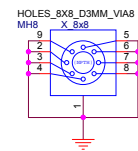
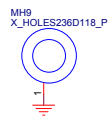
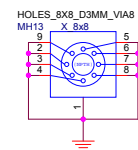
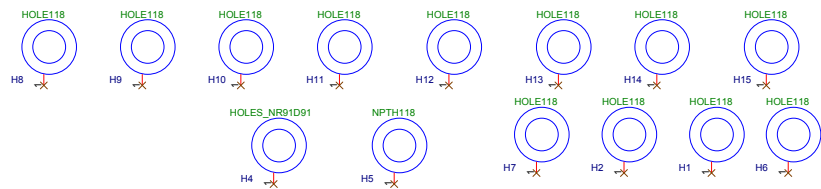


## 40 OHM

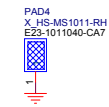
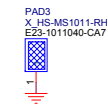
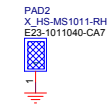
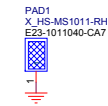
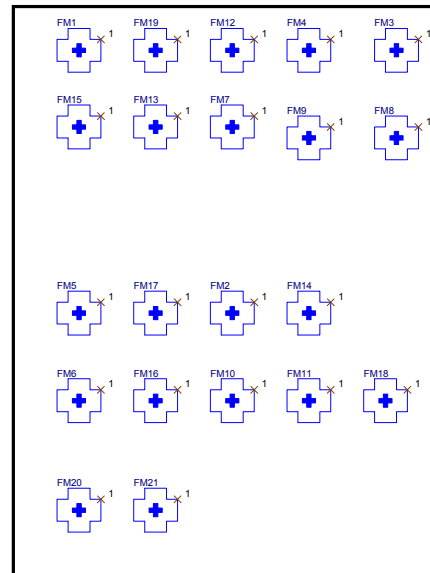


## 50 OHM

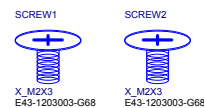
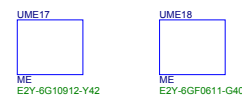




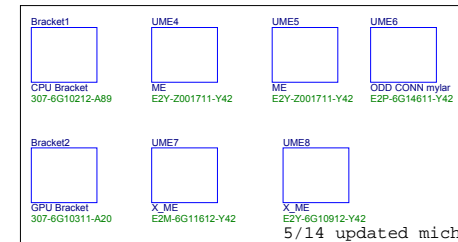
For MP: BIOS Label



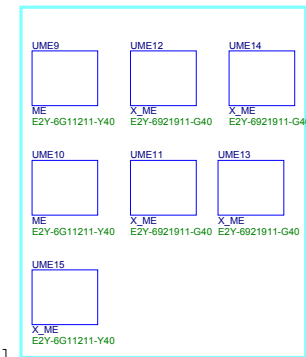
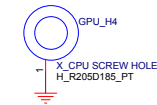
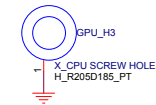
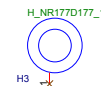
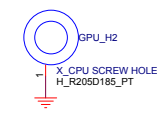
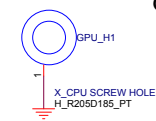
<https://vinafix.com>



04/20  
ADD SB Heatsink and Screw x2



GPU



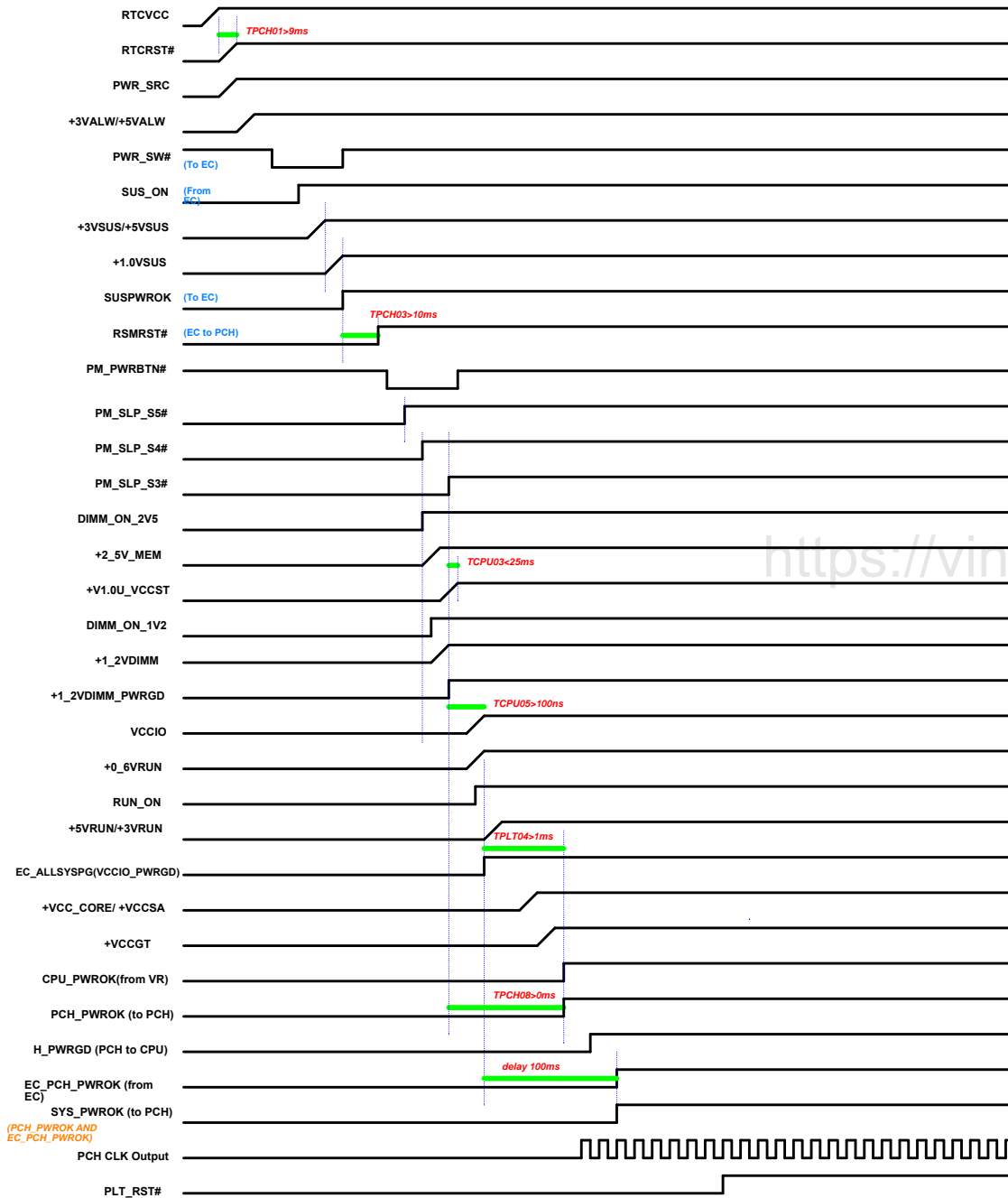
5/14 updated michael

Title		
Screw/ME		
Size	Document Number	Rev
Custom	MS-16GJ	10
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# Power on Sequence

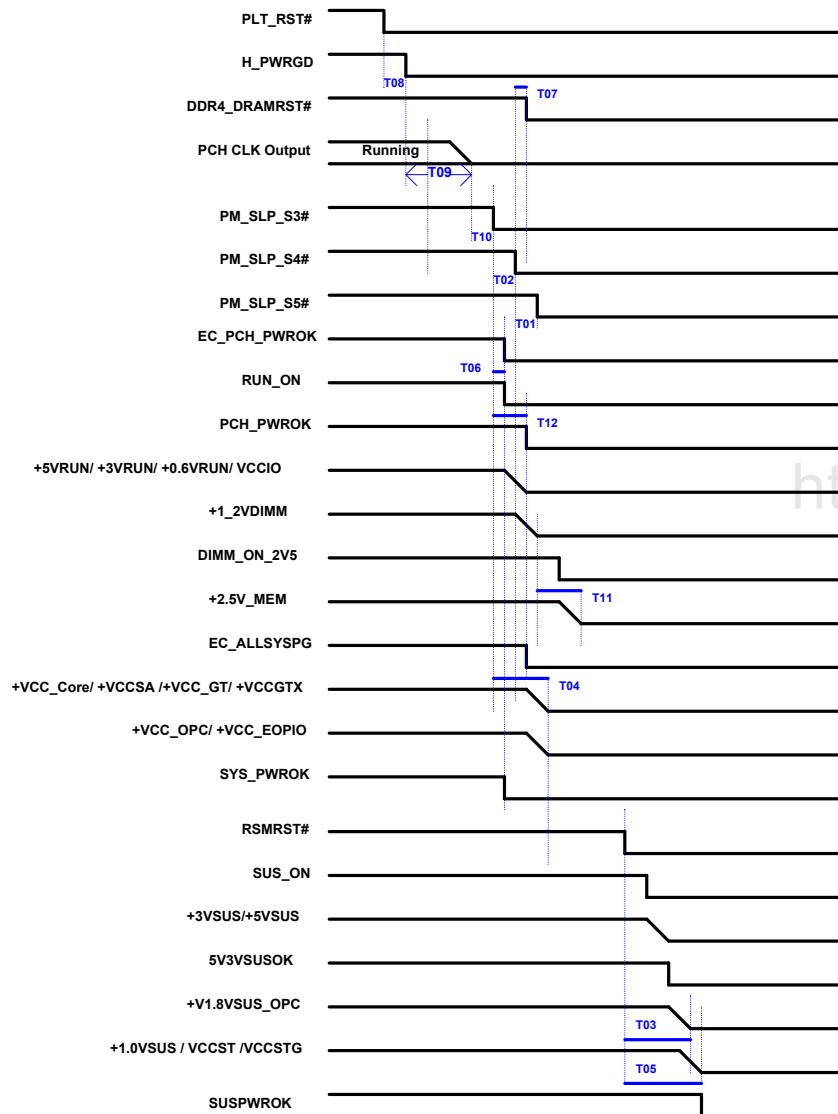
G3 -> S0



<https://vinafix.com>

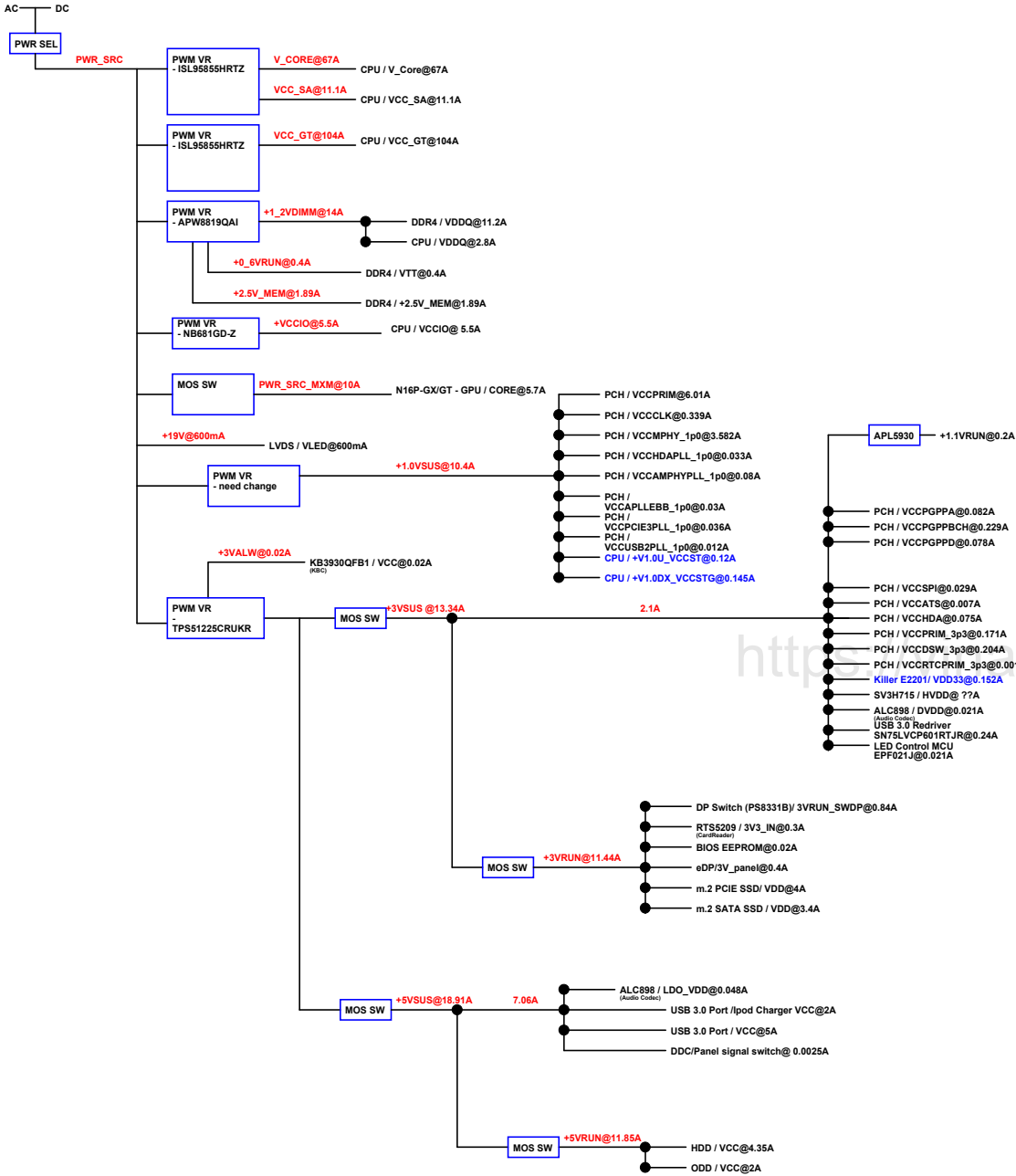
# Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
T05	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	-100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF.
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWROK deassertion

MS-1782 Power Delivery Chart



# MS-1782 Power on Block Diagram

